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FREQUENCY RECEIVER DEVELOPMENT FOR THE SATELLITE COMMUNICATIONS--ETC(U)
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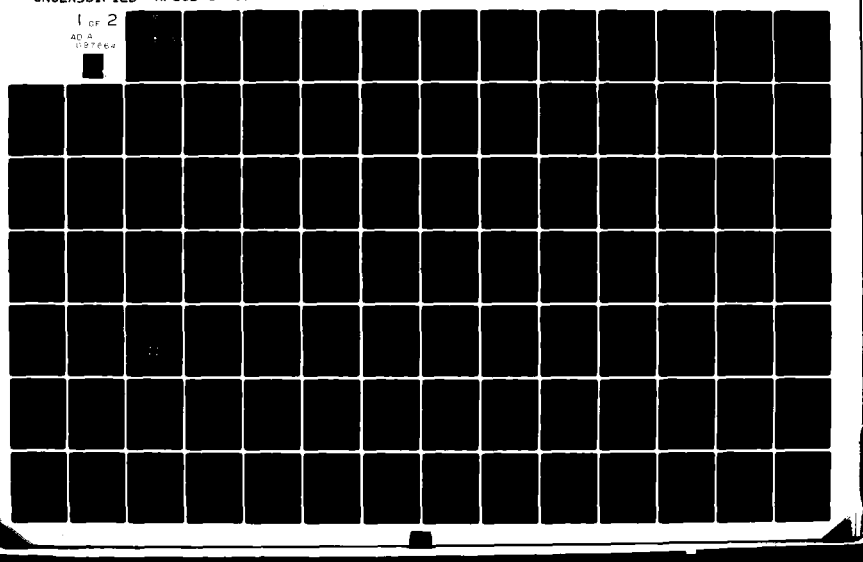

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John E. Ohlson

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Design, operation, and system integration of the Frequency Receiver portion of the Satellite Communications Signal Analyzer (SSA) are presented. This component of the SSA, which is currently under development by the Naval Postgraduate School, with the sponsorship of the Naval Electronic Systems Command, has an extensive linear dynamic processing range (of the order of 125 dB), measures the carrier frequency of received signals

with great accuracy (+/- 1 Hz), and displays the received signal in vector format. Also presented are details on receiver alignment, theory of operation, receiver parts list, receiver module descriptors and construction details. The Frequency Receiver, as one component of the SSA, will be used to assist in the management of communications traffic via Navy satellites and the performance of some radio frequency interference (RFI) functions.

ABSTRACT

Design, operation, and system integration of the Frequency Receiver portion of the Satellite Communications Signal Analyzer (SSA) are presented. This component of the SSA, which is currently under development by the Naval Postgraduate School, with the sponsorship of the Naval Electronic Systems Command, has an extensive linear dynamic processing range (of the order of 125 dB), measures the carrier frequency of received signals with great accuracy (+/- 1 Hz), and displays the received signal in vector format. Also presented are details on receiver alignment, theory of operation, receiver parts list, receiver module descriptors and construction details. The Frequency Receiver, as one component of the SSA, will be used to assist in the management of communications traffic via Navy satellites and the performance of some radio frequency interference (RFI) functions.

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TABLE OF CONTENTS

I. GOALS AND INTRODUCTION- - - - - - - - - - - - - - - 9

A. OVERVIEW- 10

B. RECEIVER IMPLEMENTATION REQUIREMENTS- - - - - 11

C. GENERAL IMPLEMENTATION- - - - - - - - - - - - 12

II. FUNCTIONAL BLOCK DESIGN AND DISCUSSION- - - - - - 13

A. FREQUENCY RECEIVER AMPLIFIER - FRA- - - - - - 13

B. FREQUENCY RECEIVER - PHASE LOCK LOOP - FRP- - 15

C. RECEIVER INTERFACE XY SWITCH - RIX- - - - - - 22

D. XY DRIVER - XD- - - - - - - - - - - - - - - - 22

E. MODULATION DISPLAY - MD - - - - - - - - - - - 22

III. DETAILED DESCRIPTION AND EXPLANATION- - - - - - - 26

A. FRA - 26

B. FRP - 32

C. XD - 44

D. MD - 45

IV. UTILIZATION OF THE HARDWARE - - - - - - - - - - - 46

A. FR PANELS - - - - - - - - - - - - - - - - - - 46

B. RI & CI INTERFACES- - - - - - - - - - - - - - 49

C. XD/MD - 49

D. FC - 50

E. OPERATOR INTERFACE- - - - - - - - - - - - - - 50

V. CONFIGURATION UTILIZATION AND TESTING - - - - - - 51

A. SYSTEM ALIGNMENT- - - - - - - - - - - - - - - 51

B. SYSTEM OPERATION- - - - - - - - - - - - - - - 53

VI. CONFIGURATION VALIDATION- - - - - - - - - - - - - 58

VII. CONCLUSIONS - - - - - - - - - - - - - - - - - - - 70

VIII. APPENDICES

A. SCHEMATICS/BLOCK DIAGRAMS - - - - - - - - - - 71

B. PINOUTS OF ASSEMBLIES - - - - - - - - - - - - 94

C. CABLING - - - - - - - - - - - - - - - - - - - 101

D. PARTS LISTS - - - - - - - - - - - - - - - - - 103

E. ALIGNMENT PROCEDURES- - - - - - - - - - - - - 124

F. NOMINAL OPERATING CONFIGURATION AND NOMINAL OPERATING LEVELS- - - - - - - - - - 130

G. COMPUTER MENUS- - - - - - - - - - - - - - - - 132

H. MODULE SUMMARY- - - - - - - - - - - - - - - - 145

LIST OF REFERENCES - - - - - - - - - - - - - - - - - - 160

INITIAL DISTRIBUTION LIST- - - - - - - - - - - - - - - 161

LIST OF FIGURES

Figure 1 - System Configuration- - - - - - - - - - - - - - 14

Figure 2 - FRP Modules, Acronyms and COAX Connections- - 16

Figure 3 - MD Display- - - - - - - - - - - - - - - - - - 24

Figure 4 - MD Display Showing CW, QPSK, BPSK, and Noise- 25

Figure 5 - 29 MHz IF Stage - - - - - - - - - - - - - - - 27

Figure 6 - Full Scale Signal Ranges- - - - - - - - - - - 29

Figure 7 - 1 MHz IF Stage- - - - - - - - - - - - - - - - 30

Figure 8 - Triangular Wave Generation Circuit- - - - - - 39

Figure 9 - FRA Layout- - - - - - - - - - - - - - - - - - 47

Figure 10- FRP Layout- - - - - - - - - - - - - - - - - - 48

Figure 11- BPSK Modulation Display, BPSK With Interference- - - - - - - - - - - - - - - - - - 55

Figure 12- Open Loop MD Display-Circle and Almost Stationary- - - - - - - - - - - - - - - - - - 56

Figure 13- Received Power Level vs. Bandwidth For Ten Degree Phase Error- - - - - - - - - - 63

LIST OF TABLES

Table 1 - FRA RF Gains - - - - - - - - - - - - - - - - - - 31

Table 2 - FRPR Reference Frequencies - - - - - - - - - - 42

Table 3 - Frequency Receiver Noise Jitter Data - - - - - 60

Table 4 - Signal Level for 30% Reduction of Loop Bandwidth- 65

Table 5 - Loop Acquisition Time- - - - - - - - - - - - - 66

Table 6 - Frequency Receiver VCXO Stability- - - - - - - 68

I. GOALS AND INTRODUCTION

The Frequency Receiver (FR) is one of the functioning receiver modules of the Satellite Communications Signal Analyzer (SSA). Design of the SSA was initiated in January 1978 [Ref. 1, 2]. A significant portion was completed by December 1979 [Ref. 3]. This report addresses the most recent (June 1980) iteration of the Frequency Receiver.

Initial efforts were directed to implementing the capabilities given in Reference 3 using circuits designed by the author and described in that report. This led to the construction of a prototype device and to its evaluation. Upon review of the results of that testing, (which are beyond the scope of this document) it was decided that while the conceptual approach to a Frequency Receiver implementation had validity, the actual circuit implementation required redesign.

This document summarizes the design goals for the Frequency Receiver, presents a block diagram explanation of the final implementation, and explains engineering details. Appendices address the material required to document a production-oriented effort.

The SSA, as outlined in Reference 4, is to be a replacement for the existing Fleet Satellite Monitoring (FSM) system. As originally envisioned, capabilities were to include

monitoring and radio frequency interference (RFI) analysis. Frequency Receiver capabilities are to partially satisfy both tasks.

A. OVERVIEW

As stated in References 3 and 4, the primary purpose of the Frequency Receiver is to measure the carrier frequency of any received signal, either from a satellite or from a radio frequency interference source (RFI). An ancillary output of the Frequency Receiver is the display in an X-Y format of the demodulated signal. This vector display of the signal allows quick determination of the modulation type, i.e., CW (Continuous Wave), BPSK (Binary Phase Shift Keying), or QPSK (Quadriphase Shift Keying). As the Frequency Receiver is linear throughout the stages prior to the X-Y display, the display also is calibrated in concentric rings to facilitate signal strength measurements relative to a reference level.

An effort has been made to write this document for three levels of interest. Chapter I addresses general conceptual and implementation topics. Chapter II addresses the Frequency Receiver in a block diagram level discussion. Chapters III and IV present more specific data about circuit operation and configuration implementation. As each section has been designed to be a self sufficient reference, the reader will recognize a certain amount of unavoidable redundancy. Appendices are included as stand-alone references to the

Frequency Receivers. These references are schematics/block diagrams, assembly pinouts, panel cabling, module and panel parts lists, test procedures, nominal operating levels, computer menus, and a module summary. The module summary has been designed to assist the operator/technician as a quick reference and troubleshooting aid.

B. RECEIVER IMPLEMENTATION REQUIREMENTS

The following is a summary of Frequency Receiver operating criteria as stated in Reference 3. The Frequency Receiver is to be used to record each satellite user's discrete carrier frequency in a time division multiple access (tdma) environment of the various Information Exchange Subsystems (IXS). In addition to measured frequency as an output, there will be a vector display capable of differentiating between CW, BPSK, and QPSK signals. A design goal is for "quick" (~ 0.1 seconds) processing and "accurate" (+/- 0.1 Hz) measurement. Frequency measurement is to be achieved utilizing a Phase-Locked-Loop (PLL). Receiver dynamic range is to be 125 dB with the capability of receiving a -150 dBm signal on the weak end of the spectrum and a -25 dBm signal on the strong side. IF bandwidths are to be 30 kHz, 10 kHz, 3 kHz and 200 Hz. PLL bandwidths are to be 1000 Hz, 300 Hz, 100 Hz, and 30 Hz. Input signal modulation is to be AM, CW, BPSK, and QPSK.

The receiver operation is to be digitally controlled by control signals generated by a PDP-11/34 minicomputer in

response to an SSA operator's input. This input is to be keyed to a displayed menu which will prompt the operator through allowed operations. Output carrier frequency is to be measured by an HP 5345A Electronic Counter made by Hewlett Packard. The X-Y vector display is to utilize a Tektronix 604A Monitor.

C. GENERAL IMPLEMENTATION

The final implementation of the Frequency Receiver uses a concept outlined in Reference 3. This implementation performs linear processing in IF stages of 29 MHz and 1 MHz, filtering in a 50 kHz IF stage and then splits the signal into two separate streams for processing. One of the processing streams accomplishes carrier extraction by implementing a PLL after hard limiting; the other processing stream accomplishes linear X-Y processing. Gain control has been implemented in all three IF stages to various degrees and gain control for the X-Y display has also been implemented. All gain control, IF bandwith selections, PLL bandwidths, and X-Y scaling controls are implemented digitally so that the Frequency Receiver can respond to algorithms implemented in the PDP-11 in responses to operator selection of options displayed.

II. FUNCTIONAL BLOCK DESIGN AND DISCUSSION

This section describes the implementation of the Frequency Receiver at a general block diagram level. Description of the 29 MHz and the 1 MHz IF sections are highlighted. Specific tabulations of component gains and losses are listed in Chapter III.

As seen in Figure 1, the Frequency Receiver consists of two major physical components. These components are the Frequency Receiver Amplifier Panel (FRA), and the Frequency Receiver Phase Lock Loop Panel (FRP). Other smaller components are the Receiver Interface X-Y Switch (RIX), the X-Y Driver, (XD), and the Modulation Display (MD).

A. FREQUENCY RECEIVER AMPLIFIER PANEL (FRA)

The Frequency Amplifier Panel (FRA) of the Frequency Receiver interfaces with the SSA Signal Selection Unit (SSU). The inputs to the receiver are downconverted (by 180 MHz) satellite signals in the frequency range of 63 to 90 MHz. The receiver is expecting signals in the range of -25 dBm for strong signals to -150 dBm for weak signals.

The Frequency Receiver Amplifier Panel (FRA) contains the 29 MHz and the 1 MHz IF portions of the receiver. Selection of this first local oscillator (LO) frequency is an operator-required action dependent upon which

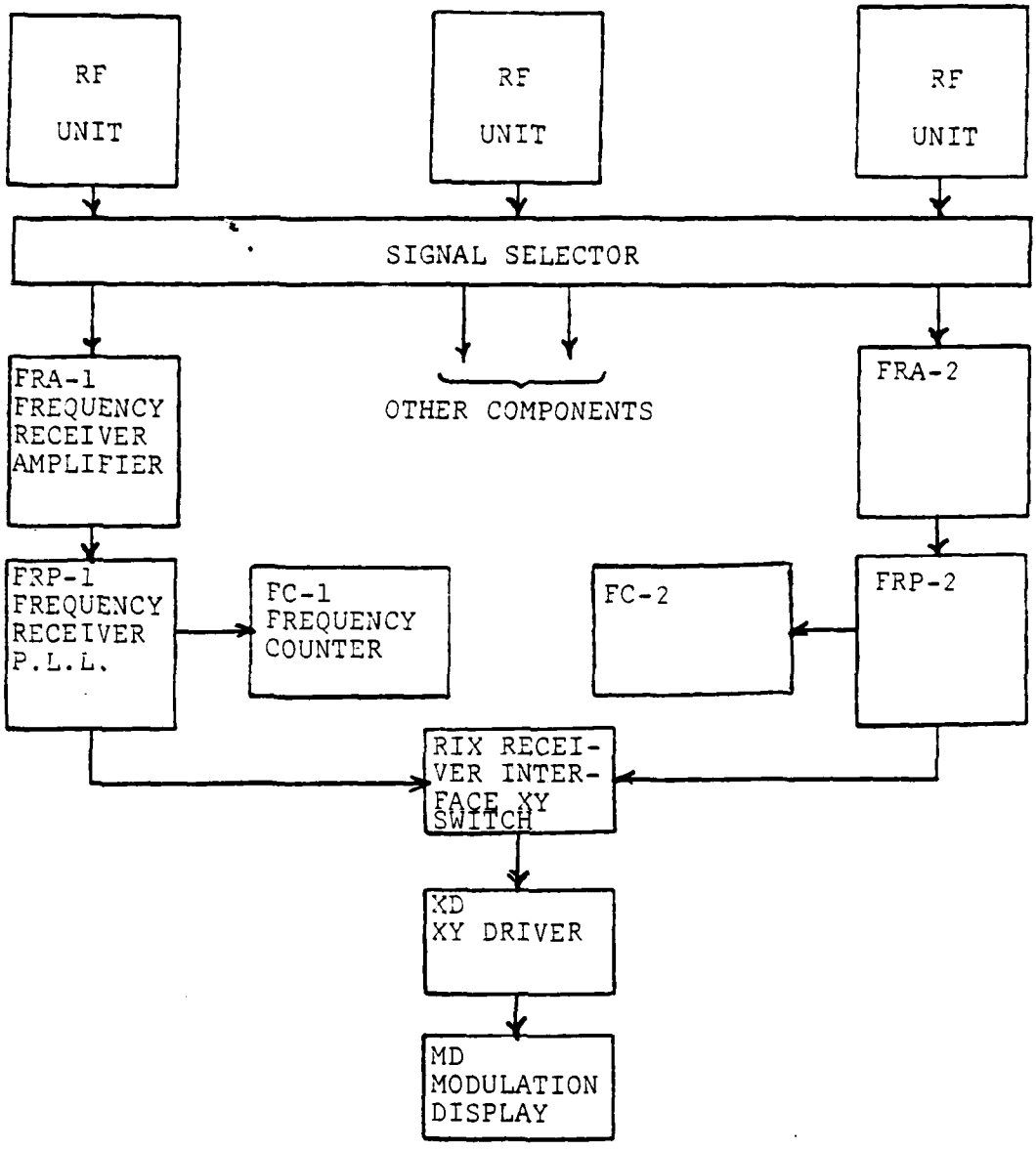


Figure 1

System Configuration

satellite signal is to be examined. This frequency is derived by the following formula:

LO(freq. in MHz) = Observed Signal (MHz) - 151 MHz

This LO frequency selection will result in an IF frequency of 29 MHz. A SSA module, the Function Generator (FG) supplies the other required LO. This LO is set for 30 MHz and is used to perform another high-side mix which results in the third IF of 1 MHz. As mentioned before, processing through this stage is required to be linear. A variable step attenuator has been inserted in the first IF section to ensure that other components are not operating in saturation. This attenuator is under computer control and may have its values changed by operator selection. Nominal signal bandwidth for the FRA is 30 kHz.

B. FREQUENCY RECEIVER - PHASE LOCK LOOP PANEL (FRP)

The second, and largest of the two Frequency Receiver panels is the FRP panel. This panel contains those portions of the receiver required to downconvert to the fourth IF (50 kHz). The FRP also searches for and locks upon a selected signal, performs carrier recovery and some portions of frequency measurements. A quadrature display is prepared in the FRP for display by other FR components. It is in the FRP that IF and Phase Lock Loop (PLL) bandwidths are selected.

The FRP is configured into physically distinct sub-modules each of which perform specified functions. Figure 2 shows the

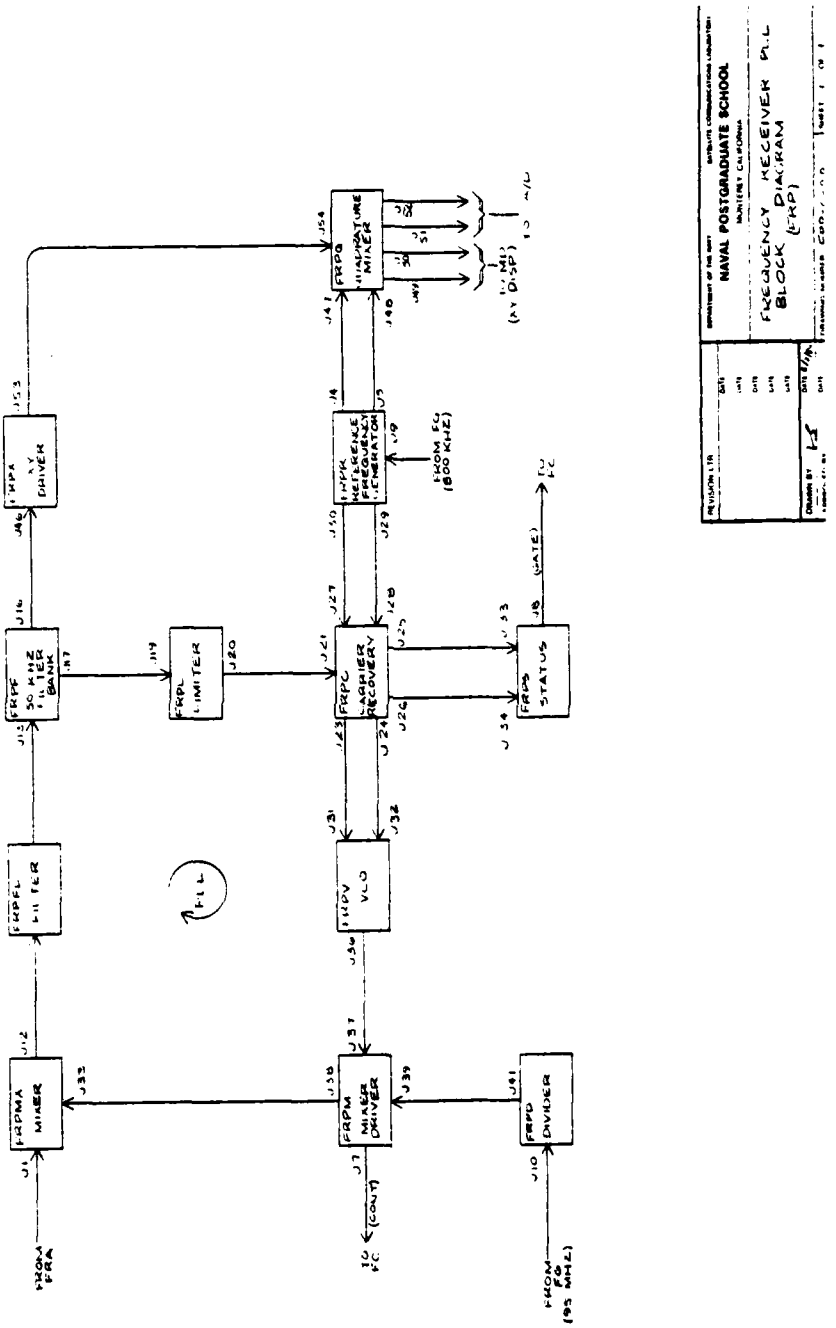


Figure 2

FRP Modules, Acronyms and Coax Connections

FRP modules, their acronyms, and the coaxial interconnections and jack numbers. These modules are:

FRPMX - FRP MIXER

FRPFL - FRP FILTER

FRPF - FRP 50 kHz FILTER BANK

FRPL - FRP LIMITER

FRPC - FRP CARRIER RECOVERY

FRPV - FRP VOLTAGE CONTROLLED OSCILLATOR

FRPM - FRP MIXER / DRIVER

FRPD - FRP 95 MHz DIVIDER

FRPS - FRP STATUS

FRPX - FRP XY AMPLIFIER

FRPQ - FRP QUADRATURE MIXER

FRPR - FRP REFERENCE FREQUENCY GENERATOR

NOTE: FRP components with a five letter acronym are commercially available components.

1. FRPMX

FRPMX is a stand alone mixer which mixes the signal presented it by FRA with a 950 kHz sinusoid presented by FRPM. This low-side mix results in the last IF of 50 kHz. FRPMX is a Mini-circuit Labs ZFM-3H mixer which has approximately a 5 dB insertion loss.

2. FRPFL

FRPFL is a K&L low pass filter with an approximate insertion loss of 0.6 dB. This filter has a 3 dB point of 1 MHz.

3. FRPF

The 50 kHz filter bank performs two functions. In this module are three filters which can be used to limit the IF bandwidth of the signal. These filters, in conjunction with a choice of no filtering give computer selectable IF bandwidths of 30 kHz, 10 kHz, 3 kHz, and 200 Hz. IF filtering in this module is accomplished in such a manner so as to ensure equivalent signal attenuation independent of the filter selected.

Computer selectable amplification is also accomplished in this module. This amplification will give a voltage gain of 53 on the output presented to FRPL and a voltage gain of 7.5 or 75 on the output presented to FRPX.

4. FRPL

The FRPL module performs hard limiting on the input signal. Gains have been adjusted to cause limiting in this module when the input signal is system noise. Also in this module is an active filter configures as a 68 kHz low pass filter. Output of this module is a 1.5 volt peak sine wave which is presented to FRPC.

5. FRPC

This Carrier Recovery module accepts the 1.5 volt peak sine wave from the limiter and reconstitutes the signal's carrier. The other required input is an appropriately selected set of reference frequencies. These reference frequencies are required in two places at a phase difference of 90 degrees.

The reconsitution is accomplished by a series of multiplications, the number of which depends upon the type of signal being reconstituted, i.e., CW, BPSK, or QPSK. This resultant carrier is compared to a reference signal to provide a lock status signal to FRPS.

6. FRPV

This module accepts phase signal information from FRPC and after loop filtering, sums the resultant voltage with a ramping potential. The ramping potential is used to augment the available error potential to expand the search range of the PLL. The resultant voltage is applied as the control voltage to a voltage-controlled-crystal-oscillator (VCXO). The presence of the ramp is dictated by the in-lock status of the receiver and is enabled by a signal received from FRPS. The ramp is enabled when the receiver is out of lock and is applied to the VCXO to cause the Frequency Receiver to search for a signal about some preselected center frequency.

This module also contains components which comprise loop filters which are digitally selectable and effect different loop filter bandwidths. The VCXO output may be applied to FRPMX to generate the 50 kHz IF.

7. FRPM

FRPM provides two functions. First, FRPM switches between the nominal 950 kHz generated by the VCXO and the more precise 950 kHz provided by FRPD for Open Loop Operation. The selected input is conditioned and subsequently provided

as an output to be applied to FRPMX. A sample of this signal is taken and provided as an output to be used in the frequency counting function of the receiver. The second function of this module is to properly condition a control bit so that it can properly drive a 0/32 dB single step attenuator in the 29 MHz IF stage of FRPA.

8. FRPD

Accepting as an input a system-provided 95 MHz sine wave signal, this module performs a division by one hundred. The resultant 950 kHz output is applied to FRPM as one of the selectable frequencies. This output is used in the Open Loop mode of operation. (A test and alignment mode of the Frequency Receiver.) Under some circumstances the output is inhibited by applying the appropriate control bits.

9. FRPS

The Status Module accepts input from FRPC and provides outputs to the X-Y display (in or not in lock), the computer (in or not in lock) and to the appropriate frequency counter (gate enable). The in lock status is also sent to FRPV and is used to disable the VCXO control ramp generator.

10. FRPX

This module conditions the 50 kHz output from FRPF and produces a usable signal for the XY display. Gain through this module is digitally controlled and is used to compensate for received signals of different levels so that they may be displayed on the MD (Modulation Display).

Adjustable in five dB steps this module can provide voltage gains ranging from 2 to 112.5.

11. FRPQ

FRPQ accepts a 50 kHz analog signal from FRPX and compares it to 50 kHz reference signals which are 90 degrees apart. The resultant signals are used in a multiplication process and subsequent filtering to derive the driving signal for the XY display. A duplicate of this signal is available as an Analog to Digital (A/D) output which may be used in future SSA configurations.

12. FRPR

The reference frequency module generates the required precise reference frequencies utilized elsewhere in the receiver. These references must not only be of the appropriate frequency, but also of the appropriate 90 degree phase relationship. Utilizing an input frequency of 800 kHz TTL provided by the SSA this module generates two 90 degree shifted sets of reference frequencies. Choice of the appropriate frequency is dependent upon the type of modulation expected. When a QPSK signal is selected a 200 kHz set of frequencies is generated. 100 kHz frequencies are generated for PSK signals and 50 kHz frequencies for CW signals. Outputs are to FRPC and to FRPQ.

C. RECEIVER INTERFACE-X-Y SWITCH - RIX

The RIX is a module which resides on the Receiver Interface (RI). This module selects the X-Y output from one of the computer selected Frequency Receivers for the XD and MD. Besides this switching function, RIX also performs some Control Bus decoding for the Frequency Receiver. This decoding includes Frequency Receiver 1 or 2 selection. This module also provides the current drive for the XD LED displays.

D. X-Y DRIVER - XD

The X-Y driver is a contiguous part of the MD. This module performs impedance matching and power division for the selected X-Y signal. The XD also interfaces this selected signal with the multipin of the MD. The final function of XD is to display which of the Frequency Receivers has been selected and to display which of the Receivers is currently in the in-lock status. This is accomplished by turning on LED's on the MD front panel.

E. MODULATION DISPLAY - MD

The Modulation Display is a Tektronix 604A Monitor with Options 4 and 6. This device has been converted into an X-Y video monitor via internal switch and strap selectable options. The MD display face has been locally fabricated and is comprised of a series of concentric circles the radii of which correspond to five dB decrements down in strength from a

signal reference. Figure 3 shows this display face. Figure 4 shows the type of display which is to be associated with each of the modulation types and noise. Amplitude modulation can be descriminated when the modulation "balls" move along one of the allowed radial components. Frequency modulation or analog phase modulation can be discerned by observing an "arcing" of the modulation "balls" about one of the allowed radial components.

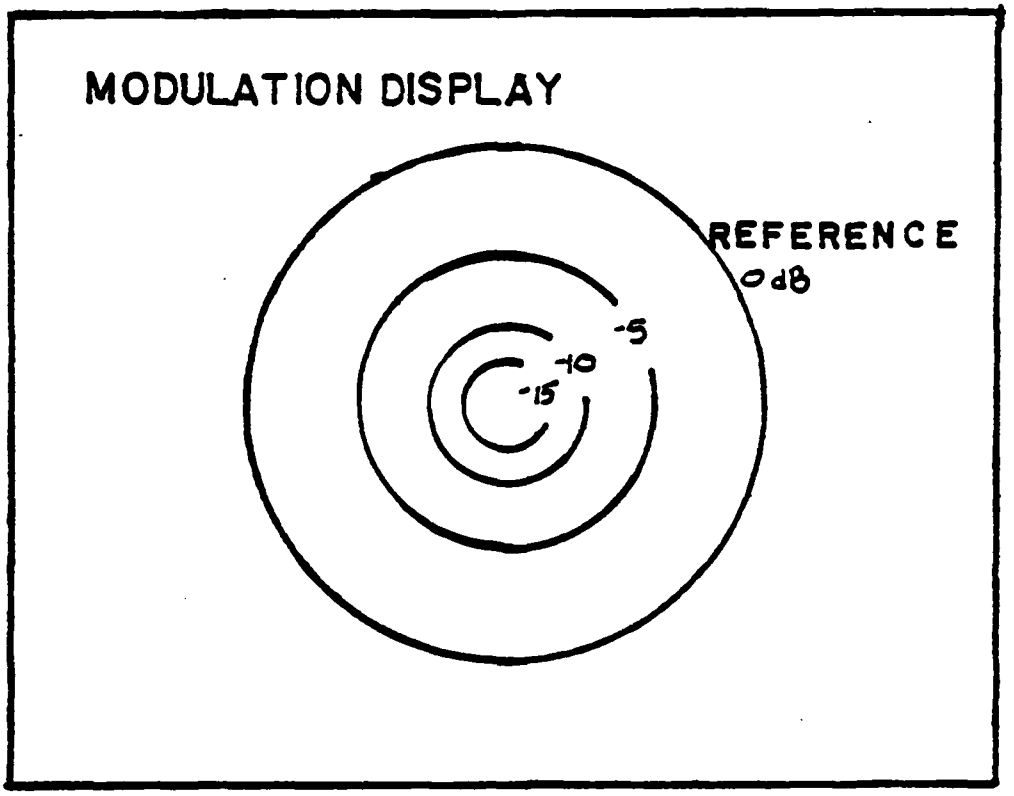


Figure 3
MD Display

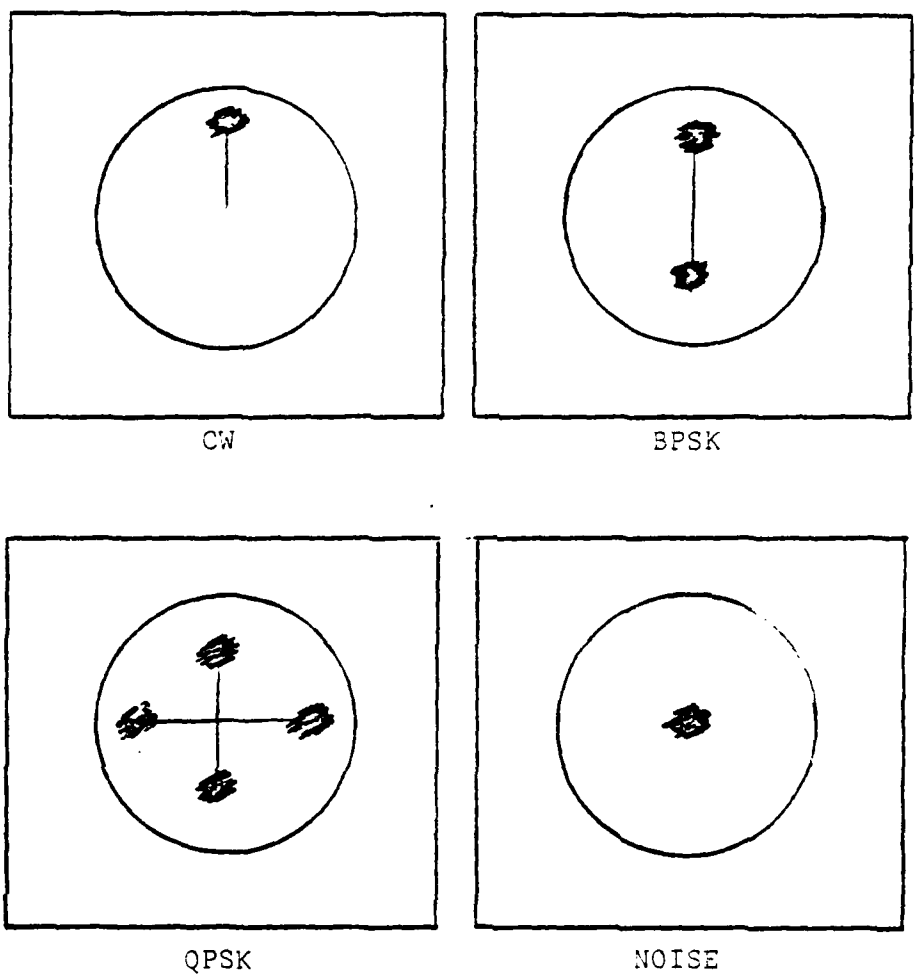


Figure 4
MD Showing QPSK, BPSK, CW and Noise

III. FREQUENCY RECEIVER DETAILED DESCRIPTION AND EXPLANATION

In this section each major component of the Frequency Receiver configuration is discussed in more detail. Gains and losses are tallied, specific circuits and interfaces are presented, and the theory of operation is presented. Presentation is in the same order as the prior section, i.e., FRA, FRP, RIX, XD, and MD. Circuits not illustrated within this section are available in Appendix A.

A. FREQUENCY RECEIVER AMPLIFIER - FRA

1. 29 MHz IF Section

Figure 5 shows the 29 MHz IF section in block detail. This chain is substantially that which was designed and presented in Reference 3. Note that filters have been inserted in this IF path in positions to assure that no feed-forward of undesired mixing products can take place. That is, amplifiers with substantial gain are separated from prior and subsequent mixers by attenuators and filters.

In Reference 3, design considerations led to a stepped Manual Gain Control (MGC). Therein, three signal ranges were created. Calculations were made to assure that when signals were received within these ranges that linear X-Y processing was accomplished. Strong signals outside of this range are displayed by the MD as distorted images. This is an indication

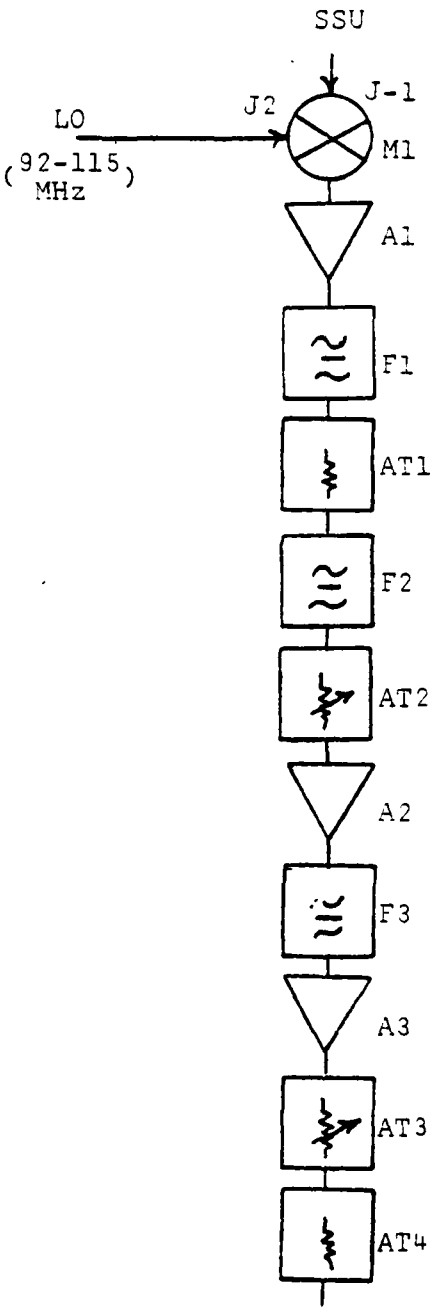


Figure 5
29 MHz Stage

to the operator to manually insert IF attenuation. When weak signals outside the range are received, a small pinpoint display allerts the operator to either remove some attenuation or change to another range. Figure 6 shows these signal ranges and their interrelationship. This stepped MGC is accomplished by TTL switching of the two DAICO attenuators shown in Figure 4 and Figure 7. Control bit discussion has been deferred until a later section.

2. 1 MHz IF Section

Figure 7 shows the 1 MHz section. This section is a deviation from the design in Reference 3. A change from integrated circuit 1 MHz processing in the prior design to one of RF component mixing and processing has been made. This transition was required partially because of significant crosstalk in the prototype 1 MHz stage when devices were implemented as IC's on a multi-function printed circuit board. Table 1 gives the gain tally by component for the 29 and 1 MHz stages.

3. FRA Alignment

The single alignment feature in the FRA is the ARM-1 variable attenuator in the 1 MHz portion. This component should be used to perform a one-time alignment of the FRA when in its nominal operating mode with the FRP with which it is to operate. Access the output of FRPFL in the FRP panel while injecting a -55 dBm test signal into the SSU at 30 MHz.

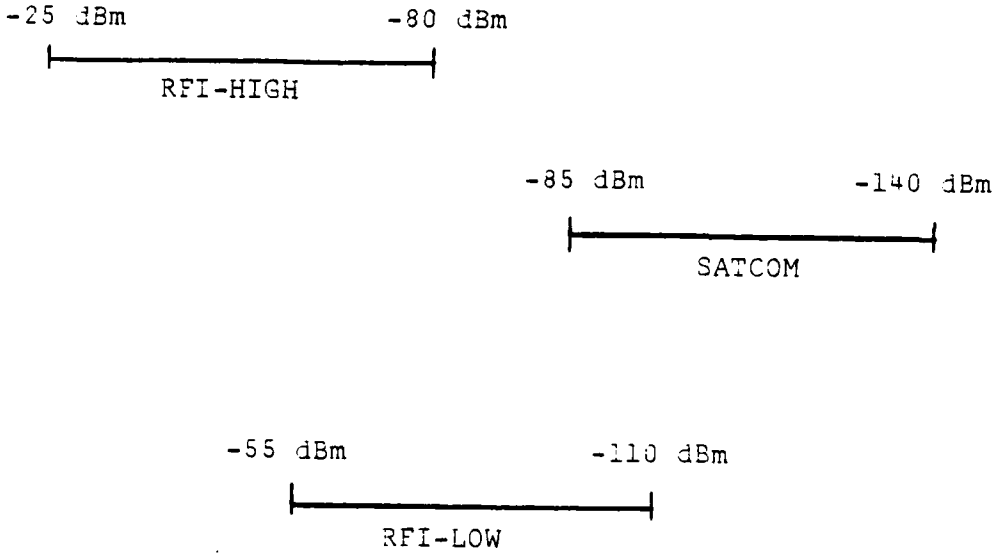


Figure 6
Full Scale Signal Ranges

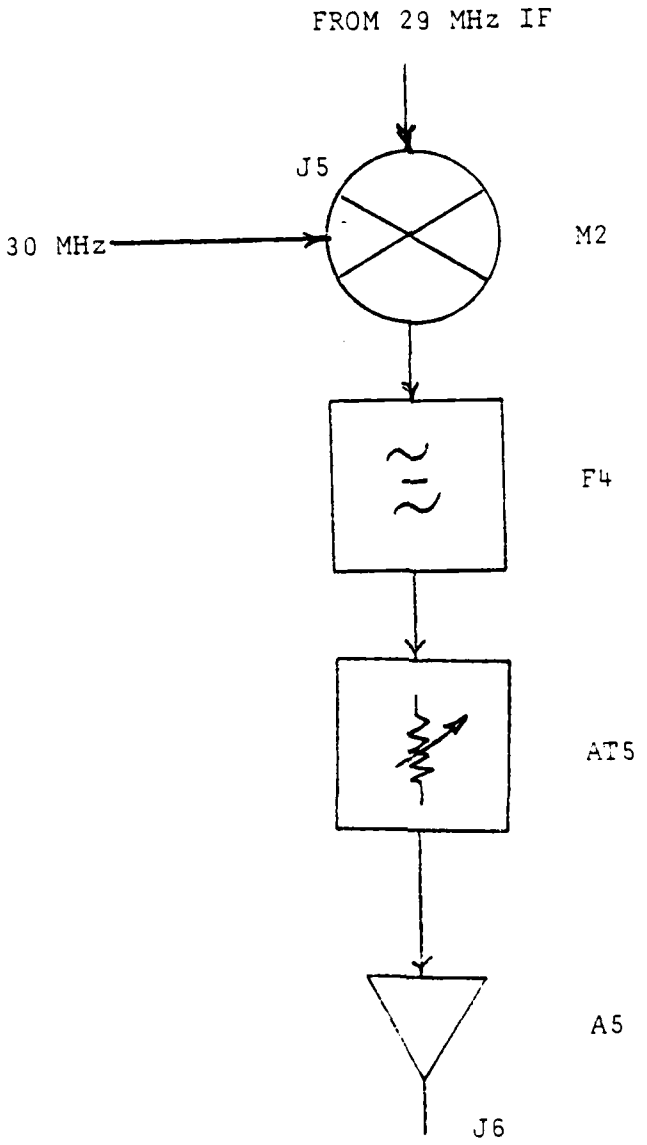


Figure 7
1 MHz IF Stage

COMPONENT		GAIN/LOSS
Mixer	M1	-8.0
Amplifier	A1	+19
Filter	F1	-5.0
Attenuator	AT1	-8.0
Step Attenuator	AT2	-3.0/-32.3 (1)
Filter	F2	-8
Amplifier	A2	+9.5
Filter	F3	-2.9
Amplifier	A3	+28.5
Step Attenuator	AT3	-2.4/-35.4 (1)
Attenuator	AT4	-3.0
Amplifier	A4	+28.5
Mixer	M2	-8.0
Filter	F3	-5.0
Variable Attenuator	ARM1	-0.3/-14.0 (1)
Amplifier	A5	+30.0

(1) Insertion Loss + (Min/Max)

Table 1

RF GAINS/LOSSES

Set the first DAICO attenuator to 0 dB and the second to 5 dB enabled. A 50 kHz sinusodal signal at -3.6 dBm (145 mv rms) should be observed across a 50 ohm load. If this value is not observed then the ARM-1 is to be adjusted to give this level.

B. FREQUENCY RECEIVER - PHASE-LOCK-LOOP - FRP

The Frequency Receiver - Phase-Lock-Loop (FRP) panel contains the "heart" of the FR; the Phase-Lock-Loop (PLL) and the associated modulation display components; FRPX and FRPQ. The PLL is composed of seven modules; FRPMX, FRPFL, FRPF, FRPL, FRPC, FRPV, and FRPM. Figure 2 shows these modules in their relative positions in the PLL. The appendix contains schematics and block diagrams for all FRP modules.

1. FRPMX

FRPMX, the stand alone mixer on the FRP panel, is presented the down converted 1 MHz IF from FRA. This signal is mixed with a nominal 950 kHz signal output by FRPM, the Mixer Driver. The resultant signal is bandlimited to a nominal center frequency of 50 kHz by FRPFL, a stand alone low pass filter.

2. FRPFL

This filter is inserted in the IF chain so as to select the desired mixing product and to separate any higher order frequency components from subsequent stages. The 50 kHz signal that results from this mix is applied to FRPF.

3. FRPF

FRPF, the 50 kHz Filter Bank, performs IF bandwidth switching for the receiver. In this module are three filters which are selected digitally by control bits. One control bit activates the relay K1 in FRPF and switches between those filters that are internal to the module and the Comstron Model FA 2594 filter which is external to it. After the signal has had the IF bandwidth limitation, it is split into two paths. One of these paths goes through a fixed gain amplifier and is passed onto FRPL, the limiter. The other signal path is through an amplifier with a choice of two values of gain. Its output then goes to the XY amplifier FRPX. This amplifier's gain is changed in FRPF by switching different value resistors into the feedback path of an operational amplifier. Voltage gain for the forward path to FRPL is 53. Voltage gain for the path to FRPX is either 7.5 or 75.

4. FRPL

FRPL, the FR limiter, is the next stage to receive the signal. Because of the particular application envisioned for the Frequency Receiver, where there is a potential for large variations in the input signal and noise levels, the next stage of signal processing is bandpass limiting. FRPL is an implementation of a bandpass limiter.

As specified in Reference 4, this hard limiter has a bandpass (zonal) filter which will pass the signal of interest.

Thus in cases where the phase modulation rate of change is much less than the carrier frequency, or in cases of amplitude modulation, we may approximate:

$$SNR_{OUT} = k * SNR_{IN}$$

$$SNR_{OUT} = S_o/N_o$$

$$SNR_{IN} = S_i/N_i$$

$$k \tilde{=} [1 + 2\ SNR_{IN}]/[a + SNR_{IN}]$$

$$a = 4/\pi$$

where S_o is the output power in the undistorted signal, N_o is the remainder of the output power at the bandpass filter, S_i is the input signal power, N_i is input noise power, and $\pi/4 < k < 2$. At low SNR_{IN} the signal is degraded by a factor of $\pi/4$, and at high SNR_{IN} it is enhanced by about 3 dB. Thus, the output power of FRPL, when the input is an unmodulated sinusoid, is a constant independent of the input power. This is also basically true for phase modulated signals whose bandwidths are relatively small compared to the bandwidth of the bandpass filter.

FRPL consists of two operational amplifiers with shunt diodes. These devices perform the hard limiting. A DATEL active filter (FLT-U2) configured as a 68 kHz low pass filter, is the other component in this module. The output of FRPL is

a nominal 1.5 v peak when the receiver is configured in its operating environment. This constant amplitude signal is then presented to FRPC, the Carrier Recovery Module.

5. FRPC

FRPC, the Carrier Recovery Module, is tasked to reconstitute the carrier of the received signal. As the Frequency Receiver is to deal with CW, BPSK, and QPSK signals, these must be processed to remove any ambiguity in their processing in the PLL. The input signal is immediately amplified and then set through a series of analog multipliers.

Specifically, the input signal, after amplification, is squared and squared again. The input signal, its square, and its fourth power are then used as inputs to a switch which selects the direct input for CW processing, the square for BPSK processing, and the fourth power for QPSK processing.

Within the circuit, U1 receives the limited signal and amplifies it. A sample of this input is presented to U6, which acts as a selection switch to select CW, BPSK, or QPSK signals. Since the carrier is already present in CW, no further processing is required and hence this sample is made available to U6 for selection. PSK and QPSK do not normally have carrier components, hence further processing is required. U2 performs the next step of this processing by squaring the input. A sample of this is presented to U6 to be used as the BPSK signal. After an additional amplification by U1, the signal is squared for a final time to result in a quadrupling. This will complete the inputs required for U6.

After appropriate modulation mode selection, U6 outputs the signal and sends it to U4 where it is multiplied by the appropriate reference frequency, i.e., 50 kHz for CW, 100 kHz for BPSK, or 200 kHz for QPSK. This results in the phase signal required for Frequency Receiver PLL-VCO (FRPV) and is selected through U6, buffered by U7 and sent differentially. These analog processes remove the phase modulation content of the signal. Thus the signal's information content is removed. U5 performs the final multiplication required with a 90 degree shifted reference to derive the input to the Frequency Receiver Status (FRPS) module. The outputs which are applied to the FRPV module are nominally 4 v p-p for CW, 2 v p-p for BPSK, and 1 v p-p for QPSK when the VCO has been disconnected so that the loop may not lock up. The output to the Status module is nominally +2 volts dc when the receiver is in lock.

6. FRPS

The in lock signal is sent to FRPS where it is averaged by an integrating operational amplifier. The signal is next routed through an adjustable RC filter whose time constant is in proportion to the IF bandwidth selected. Finally, the signal is applied to a comparator which is set nominally to 1.75 volts. This comparator with hysteresis then provides a TTL output signal which is sent to the computer via a latched status "D" flip-flop. Also in this module is a circuit which uses this in-lock information to gate the HP 8345A frequency

counter. The latched in-lock status is updated anytime the circuit loses lock. The computer then has the most recent status to be used to ascertain if the signal lost lock during the frequency measurement process.

7. FRPV

FRPV processes the phase information which FRPC provides as an output. This phase information is sent differentially from FRPC to FRPV. FRPV contains the Frequency Receiver Loop Filters, the PLL VCXO, and a triangular ramp generation circuit.

The concept of operation is a simple one. Phase information is loop filtered to derive an error signal proportional to the amount of frequency error inherent in the present PLL mixing. This error signal is applied as control voltage to a VCXO in such a manner as to reduce the tuning error of the receiver. To enhance this typical PLL operation for situations where the receiver can detect no signal within its loop bandwidth, a triangle wave function is summed with the previously discussed phase error signal and applied as control voltage to the VCXO. Thus the VCXO will sweep through a range of frequencies which will cause the Frequency Receiver to look for a signal.

The Frequency Receiver will detect the loss of lock on a signal and clear the UNLOCK LATCH flip-flop in FRPS. This flip-flop will be set by the unlock latch reset when the FR is in lock. FRPS will also send an in-lock status

signal to FRPV. This signal will defeat the triangle waveform generator and allow the loop filters in conjunction with the VCXO to track any small signal phase variations. The VCXO output is a nominal 950 kHz when there is no control voltage present. Pains were taken to specify temperature and control voltage response linearity.

The triangle waveform generation circuit is shown in Figure 8. Utilizing an integrator as a ramp generator and a threshold detector with hysteresis as a reset circuit, this circuit has one particular notable feature. Separate components within this circuit independently control the waveform's amplitude and frequency. Thus this circuit provides the capability to independently vary the VCXO frequency at a selectable rate between selectable limits. Thus, utilizing analog switches to vary the resistive parametric components, a sweep circuit may be obtained that allows waveform magnitude to change and/or waveform slope. The frequency of the waveform is determined by C3 and the resistors selected by U5. The amplitude of the waveform is independently determined by the ratio of the resistors selected in the network controlled by U6. This circuit is switched in conjunction with the selection of loop filter bandwidth. For a bandwidth of 30 Hz a sweep rate of 126 Hz/sec (0.63 V/sec) is obtained. Other values are 100 Hz bandwidth implies 1400 Hz/sec (7 V/sec), and 300 Hz bandwidth implies 12,600 Hz/sec (63 V/sec). The output

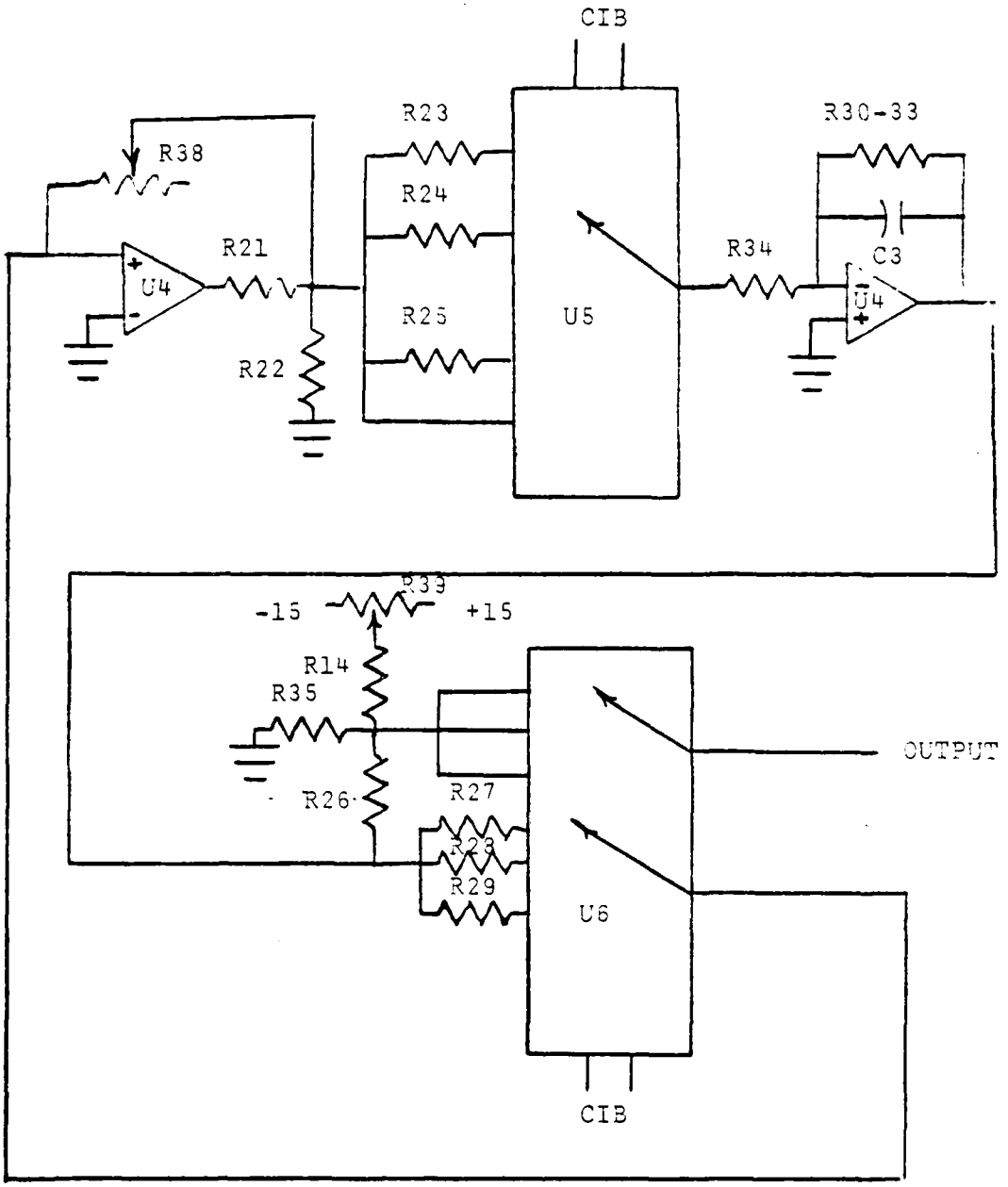


Figure 8
Triangle Wave Generation Circuit

of the FRPV module, the VCXO frequency, nominally 950 kHz, is sent to FRPM, the Frequency Receiver Mixer/Driver.

8. FRPM

The Mixer/Driver module performs two functions. Its first function is to select the appropriate input for the stand alone mixer, FRPMX. In doing so this device responds to control bits and selects a source of 950 kHz from either FRPV or FRPD. FRPV is selected for closed loop operation and FRPD is selected for open loop operation. Also performed in this module is the control bit conditioning for the Daico attenuator, AT-2. The two 950 kHz TTL inputs are switched by U1 and then driven by U2 and U3 through a transformer to match this input to FRPMX. U2 also presents a sampled version of this output to the frequency counter. An algorithm in the PDP11 will relate this sample to the center frequency of the received signal. This module completes the PLL portion of the receiver.

9. FRPD

FRPD takes as an input a 95 MHz sinusoid waveform from SSA Local Oscillator Interface and Local Oscillator 8 via the SSA Frequency Generator, and divides it by one hundred. This division is accomplished by a Plessey SP8629. U2, a 74H10, NANDs two control bits with this 950 kHz waveform. This is used as a switch to turn off the output when the OPEN LOOP mode has not been selected.

10. FRPR

The reference frequencies required elsewhere in the receiver are generated in this module. All frequencies are generated by a controlled division of the 800 kHz input. The Frequency Receiver requires two versions of each frequency derived. Each generated frequency must have a duplicate that is exactly 90 degrees out of phase. Tasked with generating 50, 100 and 200 kHz waveforms, the FRPR circuitry ensures the required phase relationships. (See Table 2)

The 800 kHz waveform is input to U1, which acts as a TTL receiver. The frequency division is performed by U2, a 7493 quad divider. The 100 kHz TTL waveform output of this division is sampled and used to trigger U3, a one shot. U3 utilizes one of three resistance values selected via control bits activating the analog switch U4. This selection in conjunction with the temperature stable capacitor determine the one shot timing. U6, a TTL switch, selects one of the available 100, 200, or 400 kHz frequencies as output and presents a sample of this selection to U7. U7 ensures that a 90 degree delay is accomplished for the selected frequency. Thus two waveforms of the selected frequency, delayed by 90 degrees are output. The other outputs of FRPR are two delayed 50 kHz waveforms. These waveforms must also have an adjustable delay relative to the reference frequencies generated above. This is accomplished by the switched monostable discussed above

CBL 13 1C1 3C1	1C2 3C2	FR1 FR2	OUTPUT FREQ (kHz)
L	L		50
L	H		100
H	L		200
H	H		200

Table 2

Freq Receiver - PLL Reference
Generator Frequency Table

above in conjunction with U5 and U8. The delay is accomplished by the potentiometers selected by U4. These potentiometers change the one shot's timing which is used to fire U5. Thus a 50 kHz TTL waveform is output which has an additional but consistent delay inserted. This adjustment will be used to rotate the decoded phase display on the MD for CW, BPSK, and QPSK separately. The outputs of 50, 100, and 200 kHz are presented to FRPC, and the 50 kHz outputs are presented to FRPQ.

11. FRPX

FRPX, the Frequency Receiver X-Y Driver, takes as its inputs one of the linearly processed and selected signals from FRPF. This input which is at 50 kHz will be a sinusoid of variable amplitude. FRPX will perform variable amplification of this signal and present this output to FRPQ. FRPX amplification selection is under operator/computer control implemented in discrete 5 dB steps by switching resistors in the feedback path of operational amplifiers.

The selected input arrives differentially, is amplified by U1, and then by U2. Selection of resistors is done again by using analog switches U3 and U4 which respond to control bits. FRPX can effect voltage gains of 2 to 112.5 which will represent ultimately observed gains on the MD of 0 to 55 dB in five dB increments. This design will ensure that linear amplification will be accomplished for a signal

up to 2.81 VRMS. The result of this signal processing is presented to FRPQ.

12. FRPQ

The Frequency Receiver Quadrature Mixer module accepts the selected reference frequencies in 90 degree shifted pairs plus the selected bandlimited linearly processed signal. Next analog multiplication and filtering is accomplished. A "slowly" varying dc signal is derived which represents the X and Y components of the vector signal. This signal is amplified and sent as an output of FRPC to the XD/MD display. The TTL reference frequency is received by U1 and passed onto U2 and U3. These analog multpliers also accept the bandlimited output of FRPX and result in a mixed output signal which when low-pass filtered by U4 and U5 (cutoff frequency = 16 kHz) become slowly varying X and Y signals respectively for XD and MD after amplification by U6 and U7. The gains U6 and U7 are adjustable so that the display on MD may be adjusted to give equal magnitudes to the X and Y components. The result of this operation is presented to XD.

D. XD

XD, the XY display driver, is a simple resistive divider. The input from FRPQ which has a full scale value of 1.7 v peak, is divided down to 0.4 v peak. This voltage is then presented to MD, the Modulation Display. XD also displays which of the two Frequency Receivers has been

selected for display by turning on one of two LED's. The lock status of each receiver is displayed by LED's.

E. MD

The Modulation Display is a Tektronix XY display. This device has a modified faceplate. Calibrated to a reference level, the MD faceplate has four concentric circles representing 0 to -15 dB levels.

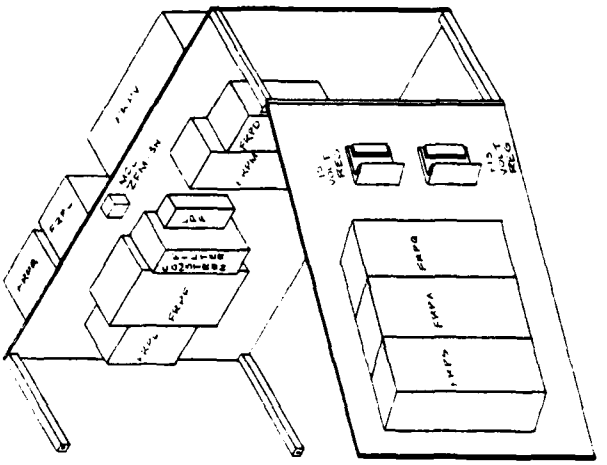
IV. UTILIZATION OF HARDWARE

This section describes the Frequency Receiver assemblies, how the two receivers are integrated into the SSA, and how they are controlled by the operator.

A. FR PANELS

The first of the two panels holds the FRA. Figure 9 shows the physical layout of this panel and the interconnection of the devices thereon. Located in a rack of the SSA this panel interfaces with the other Frequency Receiver panel, the FRP, via coax and multipin ribbon. The FRP modules are selfcontained, replaceable components. Figure 10 shows the modular arrangement to include the second level of the FRP panel. Also located on the FRP are two voltage regulators. These devices provide the +/- 15 VDC utilized everywhere in the FRP. A detailed description of these regulators is available in the appendix. Beside coaxial interconnection, there is a multipin interconnection between FRA and FRP. A mapping of this interconnection is available in the appendix. Each receiver has two coaxial lines dedicated for its respective frequency counter. These lines carry the gate enable signals to the counters and the signal to be counted.

Figure 9
FPA Layout



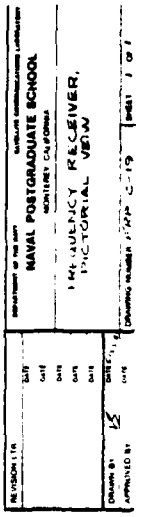


Figure 13
FRP Layout

B. INTERFACE PANELS

Communication to and from the Frequency Receiver is made via two shared multiconnector panels, the Receiver Interface (RI) and the Control Interface (CI). RI is a panel mounted in the same rack as the receivers. This panel interfaces and routes Control Bus Lines from the PDP-11 via the Control Bus to the appropriate receivers. Also through this panel pass all incoming or outgoing signals and status lines which are not coaxially run. This panel has facilities for further growth. Specifically, facilities for a future interface between the Frequency Receiver and analog to digital converters has been provided.

Also mounted on this panel is RIX, the Receiver Interface XY Switch, a component which selects which of the two FR's are to be displayed on the MD. The appendix contains the RI pinout.

Control bus interface to the Frequency Receivers via RI is made from CI, the Control Interface. Also sent to CI is the IN LOCK status for each receiver. CI routes these signals to the desired points. A mapping of the CI interface is available in the appendix.

C. XD/MD

The Modulation Display, MD, displays the vector representation of phase Modulated signals. Utilizing the Tektronix display located on the front of the SSA, this device allows

the operator to identify the type of modulation in use. Interconnection to the Frequency Receivers is via coax for the display signal and multipin connector via RI for the selection and status signals.

D. FC

The FC is the frequency counter dedicated to each of the two Frequency Receivers. These two devices are located on the front of the SSA and are normally connected to the Frequency Receivers via a coaxial connection completed on the front. These devices are available however, for other measurements by the operator. The result of the frequency measurements of the counters is sent via an HP implementation of the IEEE 488 bus to the PDP-11.

E. OPERATOR INTERFACE

All control of Frequency Receivers is made via the PDP-11 computer prompting menus. These operator-oriented CRT displays lead the operator through the sequential steps required to configure and operate the receivers. Also included in these displays are directions for configuring or modifying the Modulation Display (MD). The sole nonautomated controls in the Frequency Receiver configuration, are those associated with the MD display (ON/OFF, CENTER, etc.) and those associated with the Frequency Counter front panel. Examples of the computer menus and their software to FR hardware relationships are found in the appendix.

V. CONFIGURATION UTILIZATION AND TESTING

This section briefly addresses how the Frequency Receivers are to be utilized in conjunction with the SSA Operation. System alignment is addressed. Examples are given of the system's outputs, with a discussion as to their interpretation. Also introduced is the SSA system architecture for computer control bits.

A. SYSTEM ALIGNMENT

Ultimately the SSA will include semiautomated alignment aids. This capability is presently not available. Required for the alignment procedures in addition to the normal operating equipment is a synthesizer of 80 MHz. Also required is a spectrum analyzer, a dual trace oscilloscope, and two NAVPGSCOL "bit boxes" (devices used to simulate the PDP-11's control bits).

The control word used within the SSA is a thirty-two bit word. This word is composed of four eight bit bytes. Each word is identified in the SSA architecture by the Control Bit Latchboard (CBL) which interfaces the PDP-11's bits to the working hardware. The Frequency Receivers utilize one full CBL word, CBL13 and part of another shared CBL, CBL15. Bytes within a control word are numbered 0 thru 3. Control byte and bit documentation herein reflects those for FR1, generally.

These bytes are 0 and 1. FR2 utilizes bytes 2 and 3 of the same control word, CBL13. As the two receivers are identical in function, and interchangeable in fact, all control functions are duplicated and mirrored between bytes 0 and 1, and bytes 2 and 3. In depth documentation of the control byte/bit functions are contained in the appendix. The format for identification is, by example, CBL13-1C0 is the control bit from CBL byte one bit zero. The "C" is just a filler to make notation easier.

In general the system alignment consists of inserting the system standard alignment frequency of 80 MHz into the receiver at a known level. If the alignment signal is inserted into the Signal Selection Unit (SSU) this level is -55 dBm. With this signal present, FRA gain is set using the adjustable attenuator and measured at the output of FRPFL on FRP. This adjustment requires specified FRA attenuator settings from CBL13 and for the receiver to be in the open loop mode (using the 95 MHz provided by the SSA). With known signal level the IF bandwidth gains are set in FRPF. This requires selection of the various bandwidths and adjustment of internal variable resistors within the FRPF module. (Explicit gains and procedures appear in Appendix E.) Next, the Reference Frequency Module is adjusted. Again, requiring the selection of specified control bits and the adjustment of variable resistors within the module, this step is performed to assure the phase and frequency relationships required elsewhere.

Once the input and IF levels are established and the reference frequencies are ensured, the phase-lock-loop may be aligned. This is accomplished by validating the limited output of FRPL, and adjusting FRPC for proper reconstitution. Care must be taken in the FRPC and FRPV alignment procedures as these modules interact and form the heart of the system. After the PLL is aligned, FRPS must be adjusted to reflect the proper status for an in-lock signal. The final series of adjustments is oriented toward the system output to the Modulation Display (MD). This involves validating the input levels to FRPX when FRPF is set to provide a specified amplification upon the system standard alignment signal. FRPX is then configured to minimum gain and FRPQ is adjusted to give a specified level of 0.68 v peak output to XD. This briefly describes the system alignment procedures which are treated in greater detail in the appendix.

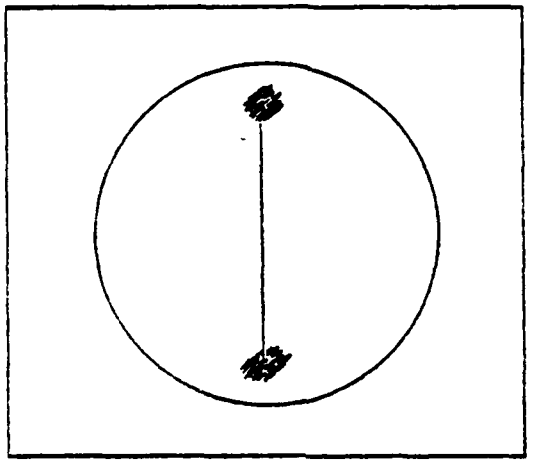
B. SYSTEM OPERATION

Once system alignment is completed and the Frequency Receivers are placed in an operating SSA, operation may commence. The normal system entry point is via the system start menu. This menu displays the many SSA functions and tasks available to the operator. The operator may select, from among these tasks, those associated with the Frequency Receiver; i.e., "FR Setup" or Modulation Display. Subsequent menus give abbreviated and detailed options. If the operator has difficulty at any level of menu, he may select a "HELP" button

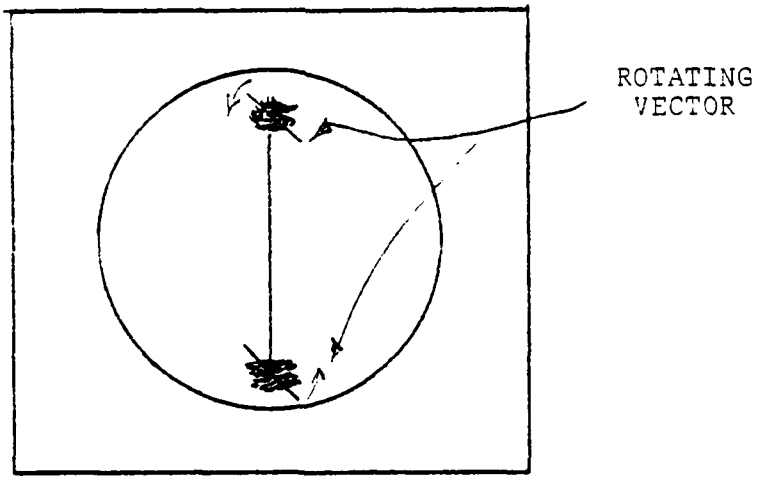
which then displays an indepth explanation. Similar steps are taken in choosing which of the Frequency Receiver's outputs are to be displayed on the MD screen. Detailed discussion of software and hardware interrelationships are available in the appendix section which addresses menus.

System outputs are of two types, a frequency measurement and a modulation display. As stated in Chapter II, the modulation display gives the operator the ability to determine at a glance the type of modulation in use on the selected channel. Figure 11a shows a typical BPSK signal. Signal strength from the reference level can be read at a glance by comparing where the modulation "balls" are in relation to the reference circle. Signal interference appears on a locked signal as a rotating vector at the end of the ball. This is depicted in Figure 11b. Any amplitude modulation on the signal will result in a radial in-out movement of the modulation "ball".

Phase stability of the transmitted signal is best observed in OPEN LOOP. In this mode, the nonsignal-coherent 95 MHz source is selected. When this is done a display similar to Figure 12a will be available. Using the offset buttons provided, the modulation rotation may be nearly stopped. Once this is accomplished, any slow rotation noted is a manifestation of phase instability of the received signal. It is necessary to make this observation in OPEN LOOP

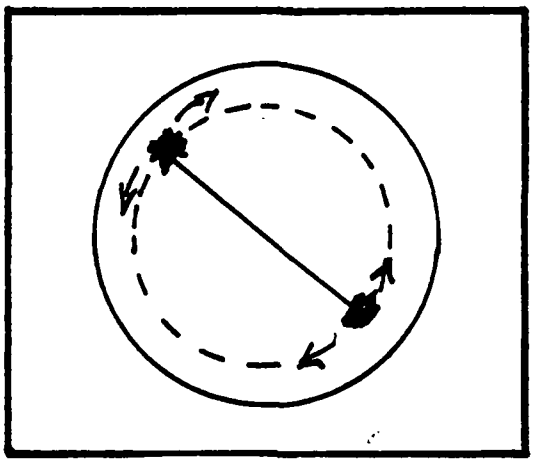


A

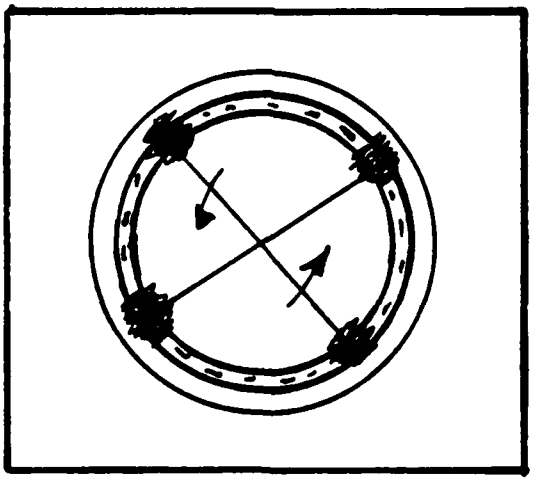


B

Figure 11
BPSK Modulation Display, BPSK With Interference



A



B

Figure 12
Open Loop MD Display - Circle And Almost Stationary

as the PLL will eliminate any small deviations of the received signal due to phase error. Frequency measurement, the other output of the receivers, is not valid during open loop measurement. Obvious also is that the receiver must be locked onto a signal before valid frequency measurement. Receiver computer protocol has been designed to assure that frequency measurements are considered valid only when the receiver is in the IN-LOCK condition and has remained so throughout the full period of the measurement. This interface is accomplished by FRPS.

VI. CONFIGURATION VALIDATION

This section presents Frequency Receiver configuration parametric validation data. Experimental data is presented and emperical observations commented upon in context with theory.

A. THEORETICAL COMMENTS

The Frequency Receiver is an implementation of a PLL with squaring and quadrupling. This PLL must operate in two modes: acquisition and track. It was observed during the receiver design that these two modes of operation invoke differences in desirable parameters. For rapid acquisition, the loop bandwidth needs to be as large as the channel noise will allow. For precise tracking, the bandwidth should be as small as oscillator instabilities allow. As Lindsey et.al. substantiates in Reference 6, if the loop bandwidth is reduced after acquisition by switching elements in the loop filter, the transients produced can bring the system out of lock. Further it has been substantiated that as signal strength varies so does PLL damping. Jaffe and Rechtin [Ref. 7] showed in 1955 that a fixed-component loop preceded by a bandpass limiter yields near-optimum performance over a wide range of input signal to noise levels. Also presented in that article were two distinct functions for loop filter design:

1. The loop filter should minimize VCO phase-noise jitter due to noise interference.
2. The loop filter should maintain, at a specified level, transient error in the VCO phase due to specified changes in signal phase.

Also in that article the authors present the disadvantages of the AGC concept of signal strength compensation and present the idea of using a bandpass limiter. They show that a bandpass limited approach injects only 15 percent greater error than an optimum loop, while the AGC approach invokes a 45 percent total error.

This iteration of the Frequency Receiver addresses each of these areas. The bandpass limiter is used in conjunction with a stepped manual gain control to reduce PLL transients due to parametric variation caused by input signal strength variations. To effect a compromise in loop filter design for response effectiveness, different loop filter bandwidths were designed and validated. These filter bandwidths are discretely selectable.

B. MEASURED DATA

Table 3 presents noise jitter validation data acquired in the laboratory. Viterbi [Ref. 5, p. 40-42] shows that as $(SNR)_{IN}$ decreases, the actual loop bandwidth decreases in receivers using bandpass limiters. This effect results in a reduction of phase-error variance in practice. As can be

FREQUENCY RECEIVER 2

B_{IF} (kHz)	B_{LOOP} (Hz)	C (dBm)	σ_{TH}: CW (deg)	σ_{QB}: CW (deg)	$\sigma=10^{\circ}$
10	100	-113.8	0.807	1	-140
		-123.8	2.55	3.25	
		-133.8	8.07	8.55	
		-143.8	25.5	21.0	
10	30	-113.8	0.44	0.57	-153
		-123.8	1.40	1.14	
		-133.8	4.42	2.28	
		-143.8	13.99	4.56	
3	1000	-113.8	2.55		
		-123.8	8.07	unstable	
		-133.8	25.54		
		-143.8	80.75		
3	100	-113.8	0.81	1.99	-133.8
		-123.8	2.55	3.99	
		-133.8	8.07	9.97	
		-.43.8	25.50	11.4	
3	30	-113.8	0.44	0.57	-152.9
		-123.8	1.40	1.03	
		-133.8	4.42	1.14	
		-143.8	13.99	3.42	
30	1000	-113.8	2.55	2.57	-130.0
		-123.8	8.07	4.28	
		-133.8	25.54	11.40	
		-143.8	80.75	22.80	
30	300	-113.8	1.40	0.68	-135.0
		-123.8	4.42	2.28	
		-133.8	13.99	3.55	
		-143.8	44.23	22.80	
30	100	-113.8	0.81	0.68	-138.0
		-123.8	2.55	2.28	
		-133.8	8.07	5.13	
		-143.8	25.50	17.10	
30	30	-113.8	0.44	0.68	-143
		-123.8	1.40	1.14	
		-133.8	4.42	2.85	
		-143.8	13.99	10.26	

Table 3

Noise Jitter

Table 3 con't

10	1000	-113.8	2.55	2.28	-125.0
		-123.8	8.07	6.27	
		-133.8	25.50	15.96	
		-143.8	80.75	28.50	
10	300	-113.8	1.40	1.37	-134.0
		-123.8	4.42	3.13	
		-133.8	13.88	7.98	
		-143.8	44.23	11.40	
.2	30	-113.8	0.44	0.46	-145.0
		-123.8	1.40	1.14	
		-133.8	4.42	5.70	
		-143.8	13.99	8.55	

seen by the data on Figure 13, this effect was validated emperically. The rms theoretical phase jitter error was calculated from:

$$\sigma_{(deg)} = \sqrt{\frac{B_L}{C/N_o}} \cdot \frac{180}{\pi}$$

Where C is the input signal strength in dBm at the antenna, N_o was taken as 600 degrees Kelvin times K, and B_L is the loop bandwidth in Hertz. The observed jitter was determined empirically by observing the output of the VCXO on an oscilloscope which was synchronized to a synthesized standard. The column titled σ = 10 degrees lists those signal levels below which an error greater than ten degrees was observed.

It is worthwhile to ascertain at what received signal power level the loop bandwidth is decreased by thirty percent. As the loop bandwidth varies approximately as the loop gain, we may write:

$$\text{Loop Gain} = \frac{1}{\sqrt{1 + \frac{1}{k\ SNR_{IN}}}}$$

Now setting the loop gain to 0.7 ;

$$0.7 = \frac{1}{\sqrt{1 + \frac{1}{k\ SNR_{IN}}}}$$

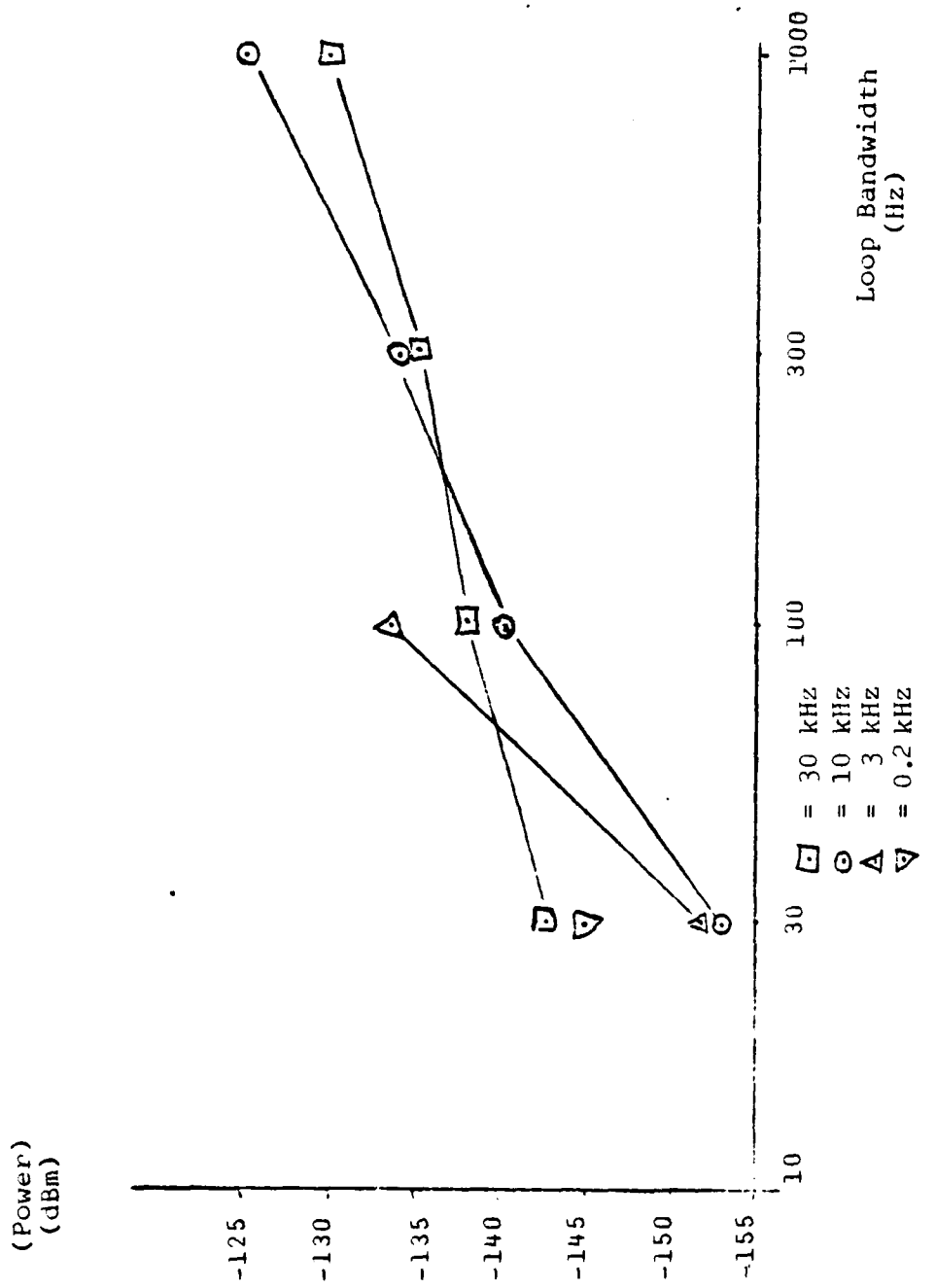


Figure 13

Received Power Level vs. Bandwidth For Ten Degree Phase Error

which can be shown to equal:

$$k\ SNR_{IN} \cong \frac{0.49}{0.51} \cong 0.96 \cong 1.0$$

Hence the input signal to noise ratio equals zero, to a first approximation, when the loop bandwidth has dropped by approximately thirty percent. Computing input signal to noise ratio:

$$SNR_{IN} = \frac{C}{kTB} = 1\ (0dB)$$

where:

k = -198.6 dBm/K-Hz

T = 600 K = 27.8 dBK

B = 0.2, 3.0, 10.0, 30.0 Hz

Thus:

$$C = -198.6 + 27.8 + 10 \log (B\langle Hz \rangle)$$

$$= -170.8 + 10 \log B$$

The results of this calculation are contained in Table 4. This table lists the signal strengths that would result in a significantly reduced loop bandwidth (and also loop gain).

Table 5 reflects data for receiver acquisition time. This data was acquired by averaging the time required for receiver lock on an input signal of a given frequency displacement while the receiver VCXO was being swept. This displacement was established above and below the nominal loop center

Signal Levels For 30%

Loop Bandwidth Reduction

B_{IF} (Hz)	C (dBm)
200	-147.8
3000	-136.0
10000	-130.8
30000	-126.0

B_{IF}= IF Bandwidth

C = Received Signal Strength

Table 4

B_{IF} (kHz)	B_{LOOP}	Δf (Hz) (1)	SWEEP (2)	$TACQ_{AV}$ (SEC) (3)
.2	30	800	1K	2.1
.2	30	160	200	1.6
10	30	800	1k	9.8
10	30	160	200	1.7
3	30	800	1k	5.3
3	30	160	200	4.4
30	30	800	1k	6.7
30	30	160	200	1.4
30	1k	800	1k	Immediately
30	1k	160	200	Immediately

NOTE:

(1) Δf represents an off center frequency deviation. 50% of data taken above and 50% taken below the center freq.

(2) Sweep is volt/sec change of VCXO control voltage.

(3) $TACQ_{AV}$ is acquisition time average in seconds from no signal to signal present.

Table 5

frequency and the measured times averaged. The frequency displacement from loop center frequency is Δf. The sweep deviation used in volts per Hertz is indicated by the SWEEP column.

Table 6 gives data for VCXO rest frequency stability. Data here was collected while the receiver was configured in all possible combinations of loop bandwidths, modulation modes, and IF bandwidths.

IF (kHz)	MODE	LOOP (Hz)	REST FR#2	FREC FR#1
30	CW	1000	949.9184	949.9971
		300	949.9868	949.9989
		100	950.0065	950.0003
		30	950.0136	950.0003
10	CW	1000	950.1756	949.9979
		300	950.0618	949.9993
		100	950.0354	949.9990
		30	950.0305	950.0004
3	CW	1000	947.8088	950.5592
		300	949.3360	950.0000
		100	950.0000	949.9999
		30	950.0000	950.0000
.2	CW	1000	950.1779	949.6969
		300	949.9345	949.7407
		100	949.7370	949.7865
		30	949.6374	949.8730
30	QPSK	1000	949.9999	950.0000
		300	950.0000	949.9364
		100	950.0000	949.9365
		30	949.9999	949.9346
10	QPSK	1000	949.9999	949.9998
		300	949.9999	949.9999
		100	950.0000	950.0001
		30	949.9999	949.9907
3	QPSK	1000	949.9997	950.0018
		300	950.0048	949.9997
		100	950.0045	950.0000
		30	950.0038	950.0000
.2	QPSK	1000	949.9474	949.8796
		300	949.9657	950.0472
		100	950.0133	950.0337
		30	950.0126	950.0317

Table 6

VCO Rest Freq Data

Table 6 con't

30	BPSK	1000	950.0193	949.9999
		300	950.0111	949.9998
		100	950.0087	949.9469
		30	950.0071	949.9627
10	BPSK	1000	950.0099	950.0002
		300	950.0075	949.9998
		100	950.0068	949.9993
		30	950.0066	950.0001
3	BPSK	1000	950.0004	949.9695
		300	950.0011	949.9910
		100	950.0052	949.9999
		30	950.0044	949.9999
.2	BPSK	1000	949.9887	950.0346
		300	950.0063	949.7406
		100	950.0237	949.8345
		30	950.0005	949.8664

VII. CONCLUSIONS

The Frequency Receivers of the SSA are valuable and versatile tools for the satellite communications link manager. These devices meet their stated objectives of carrier frequency measurement and modulation display. The full capability of the receivers will be evident when the full SSA is in operation. The receiver design followed the concept of "a defensible design". In doing so, the product should adequately stand the trial of time for component reliability. Human factors engineering was considered in the configuration layout. Certain compromises were made, however, in the interest of timely development, as the receiver's ultimate form did not take shape until the last six months.

Subsequent Frequency Receiver development will address an analog to digital interface. Physical provisions have been left in most places to accommodate expansions of this nature. Also of eventual need is the interface with the Test Unit for Frequency Receiver alignment and testing. A final and close look must also be given to parts and module placement. The second level of the FRP panel and the mechanism where it hinges from the secured plate deserves examination.

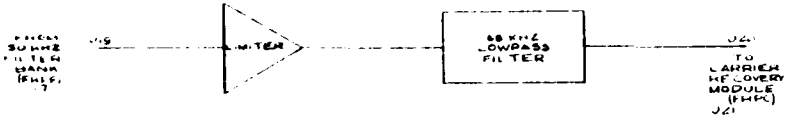
The Frequency Receivers meet their functional objectives and perform within expected tolerances.

APPENDIX A

SCHEMATICS

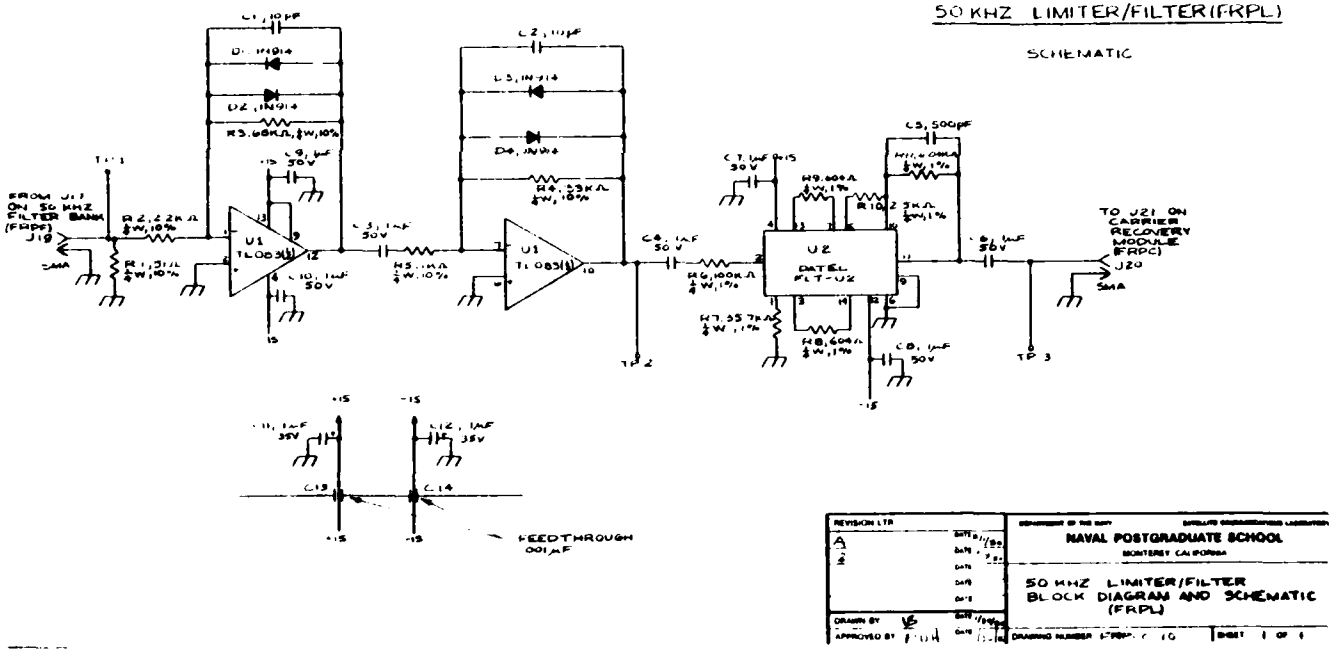
FREQUENCY RECEIVER - BLUEPRINT DIAGRAMS

This appendix contains the working schematics and block diagrams of the Frequency Receivers.



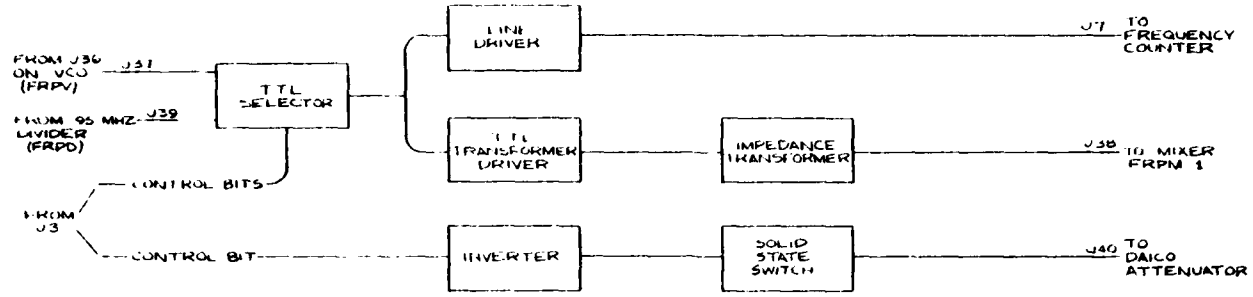
50 KHZ LIMITER/FILTER(FRPL)

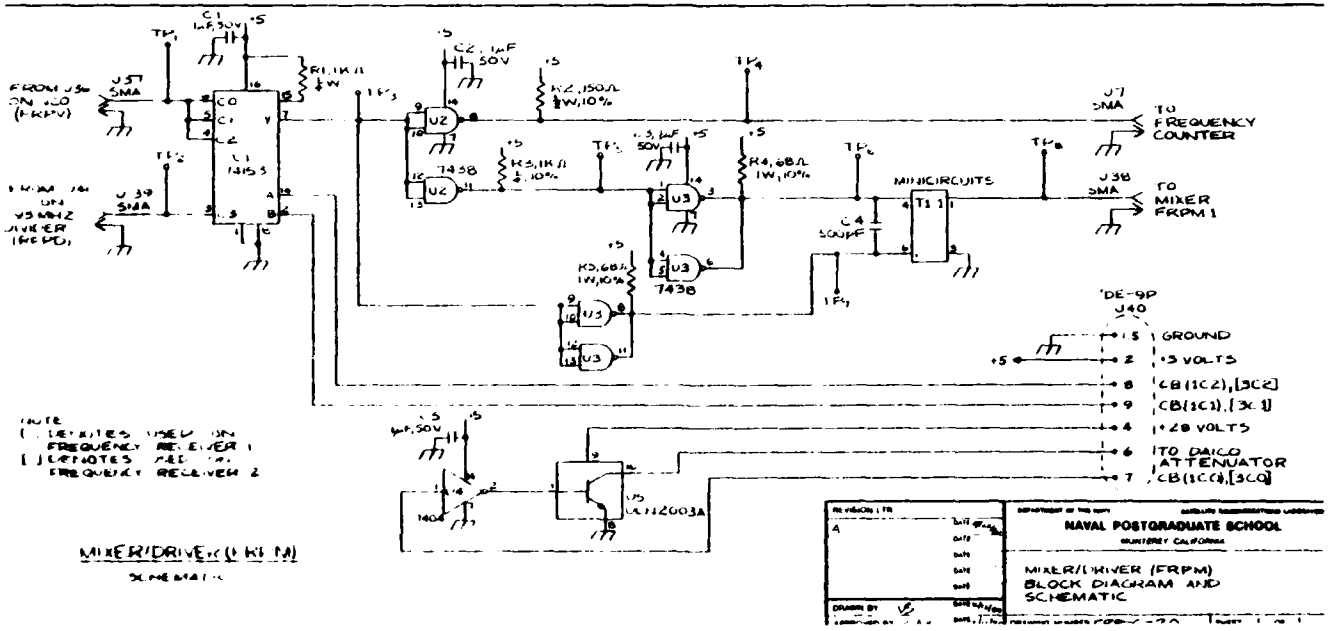
BLOCK DIAGRAM



MIXER/DRIVER (FRPM)

BLOCK DIAGRAM





MIXER/DRIVER (FRPM)

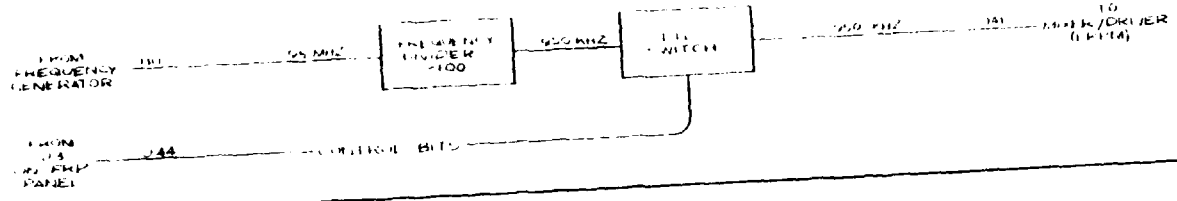
SCHEMATIC

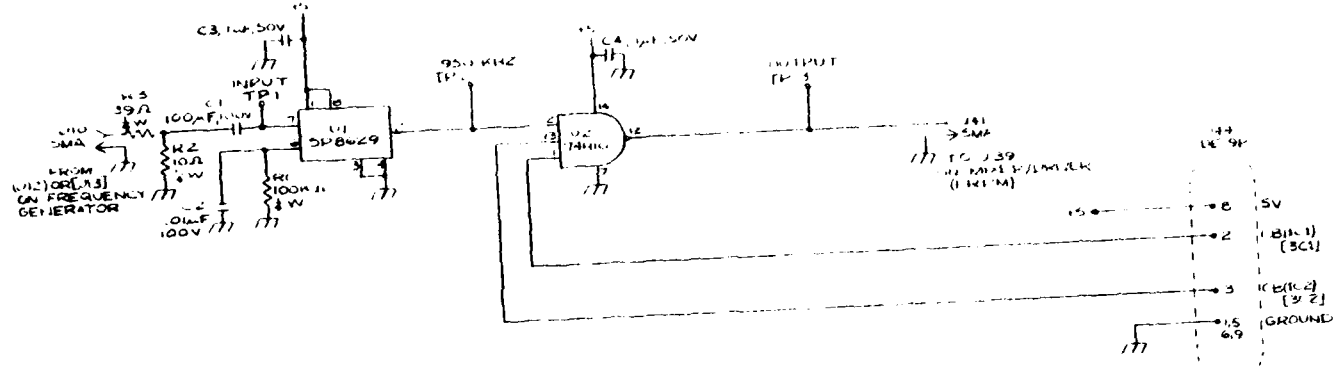
NAVAL POSTGRADUATE SCHOOL
MONTEREY CALIFORNIA

MIXER/DRIVER (FRPM)
BLOCK DIAGRAM AND SCHEMATIC

95 MHZ DIVIDER (FRPD)

BLOCK DIAGRAM



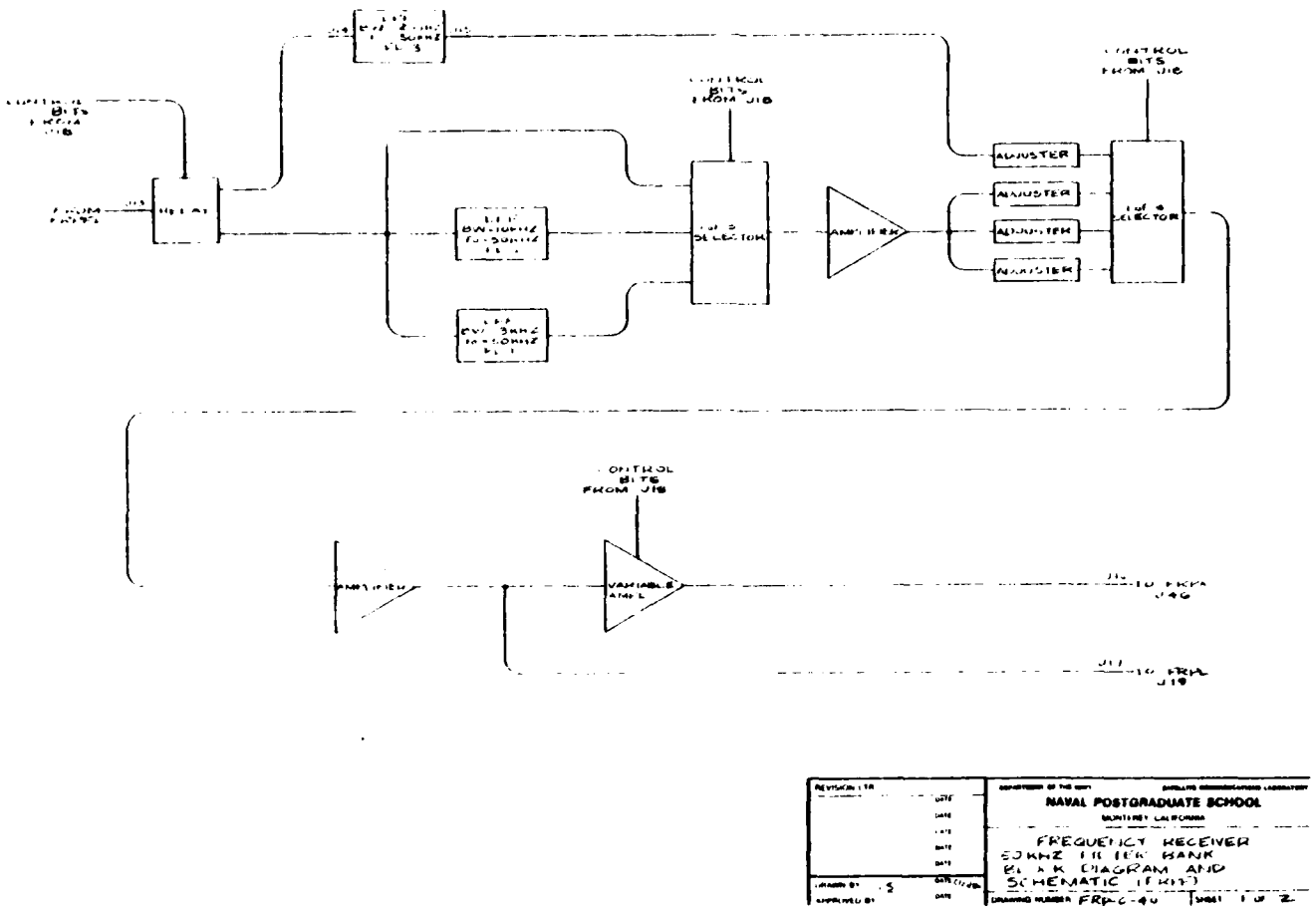


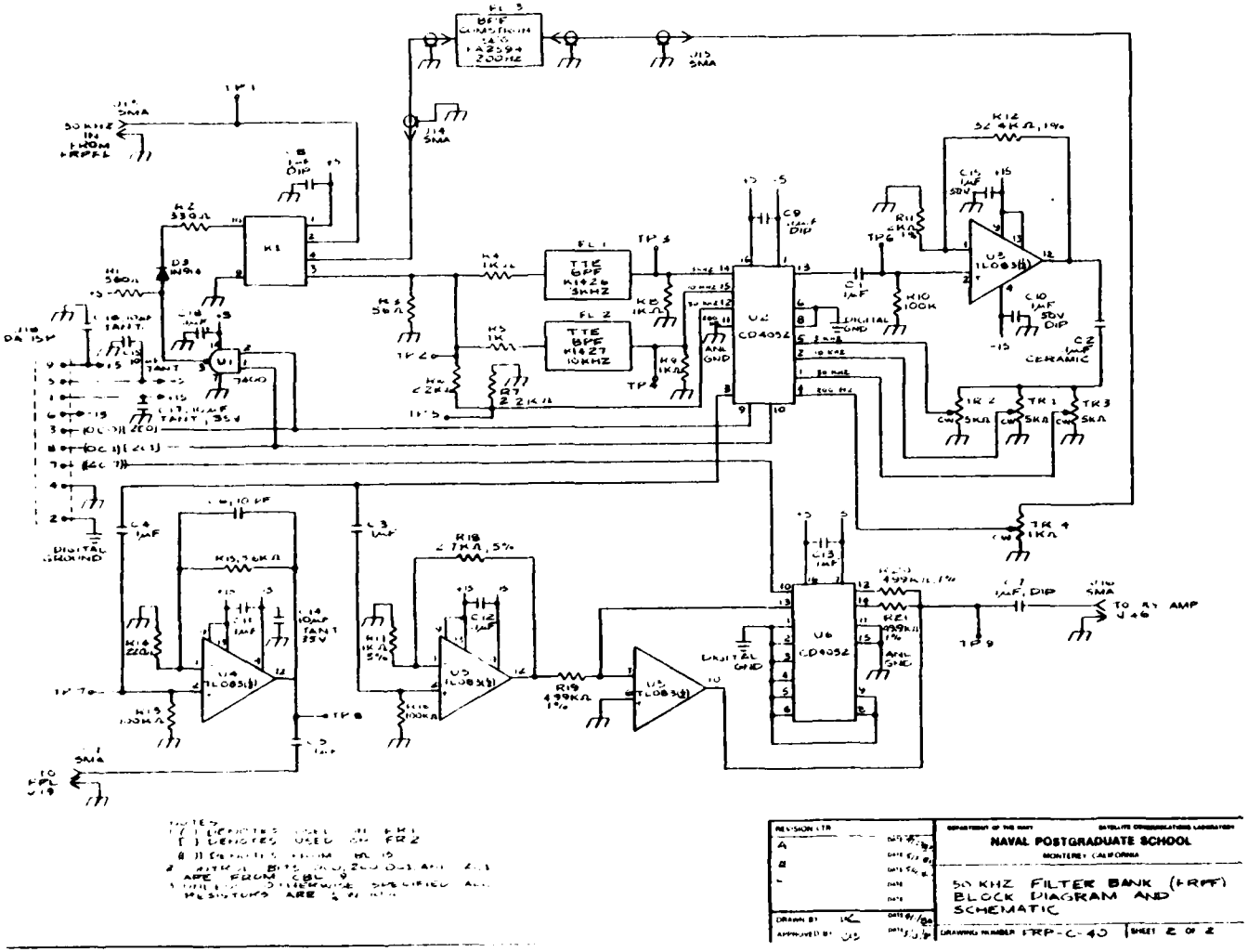
NOTE
( ) DENOTES USED ON FREQUENCY RECEIVER 1
[ ] DENOTES USED ON FREQUENCY RECEIVER 2.

95 MHZ DIVIDER (FRPD)

SCHEMATIC

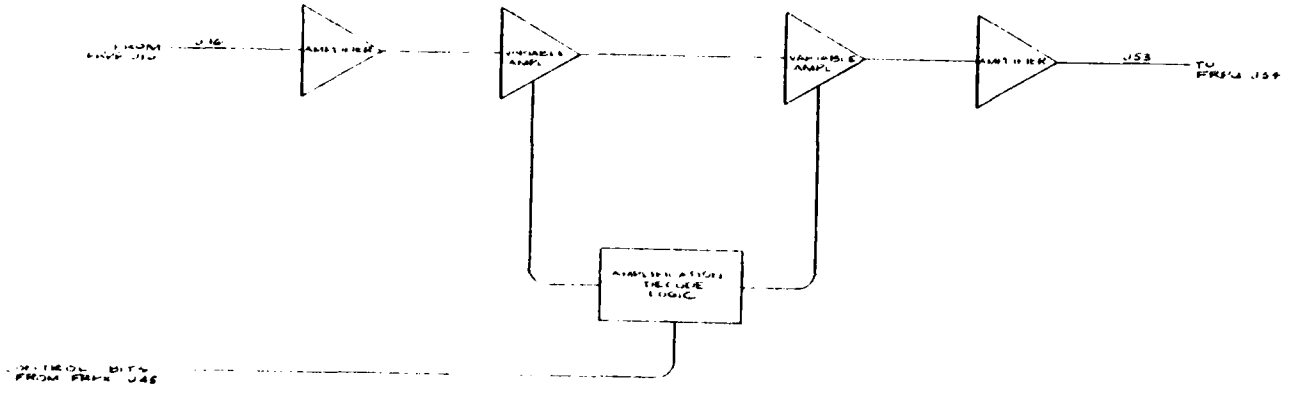
REVISION CTR	DEPARTMENT OF THE NAVY — NAVAL POSTGRADUATE SCHOOL, MONTEREY CALIFORNIA
	95 MHZ DIVIDER (FRPD) BLOCK DIAGRAM AND SCHEMATIC
DRAWN BY	DRAWING NUMBER FRP-C-30 — SHEET 1 OF 1
APPROVED BY	


CONTROL BITS FROM J18
ADJUSTER
ADJUSTER
ADJUSTER
ADJUSTER
SELECTOR
SELECTOR
CONTROL BITS FROM J18
CONTROL BITS FROM J18
VARIABLE AMPL
TO FRPA J46
TO FRPL J19
NAVAL POSTGRADUATE SCHOOL
MONTEREY CALIFORNIA
FREQUENCY RECEIVER
50KHZ FILTER BANK
BLOCK DIAGRAM AND
SCHEMATIC (FRPF)
DRAWING NUMBER FRP-C-40
SHEET 1 OF 2

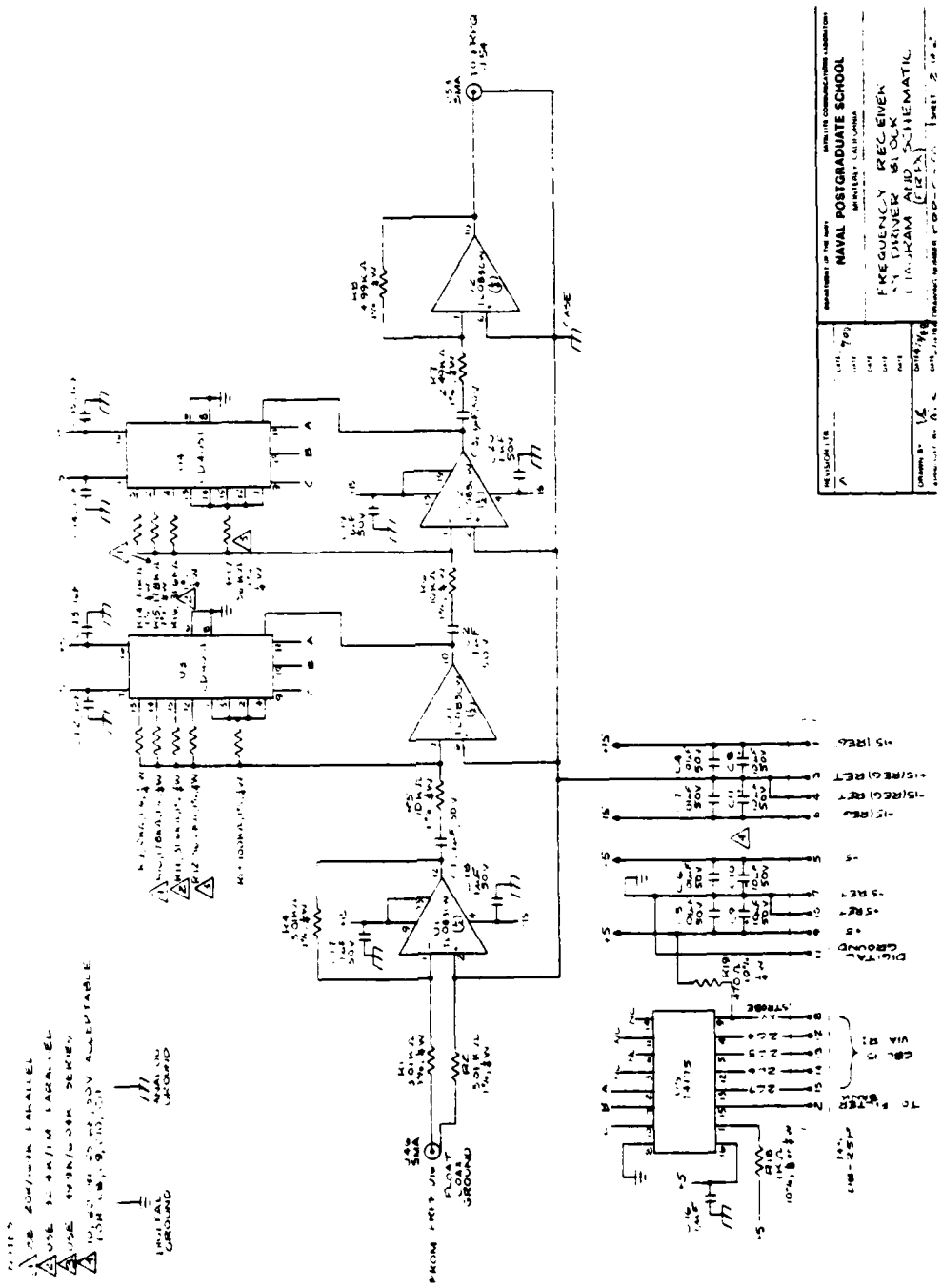


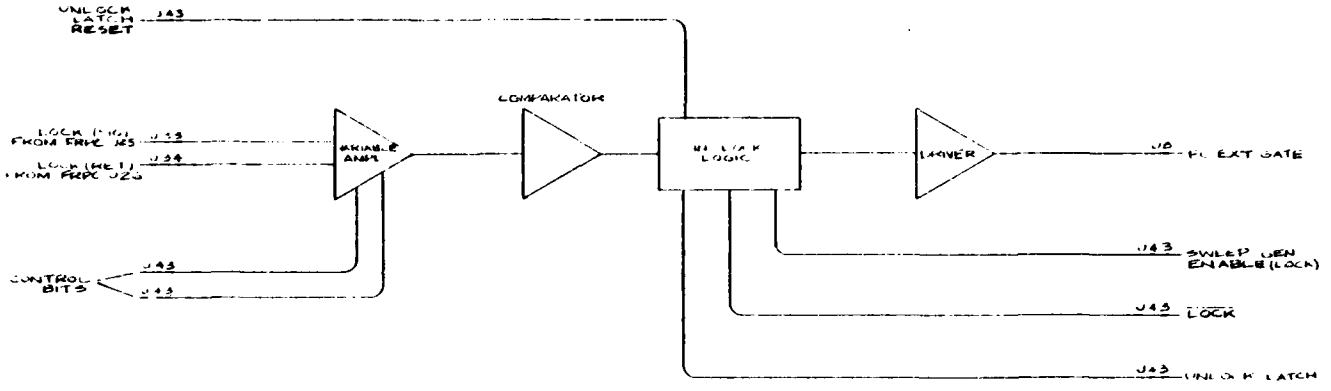
NOTES
1. ( ) DENOTES USED ON FR1
[ ] DENOTES USED ON FR2
(( )) DENOTES FROM BL 15
2. ALTERNATE BITS 200, 200 D-3 AND 2C3 ARE FROM CBL 9
3. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE ¼ W 10%

REVISION LTR		DEPARTMENT OF THE NAVY — SATELLITE COMMUNICATIONS LABORATORY
A	DATE	NAVAL POSTGRADUATE SCHOOL
B	DATE	MONTEREY CALIFORNIA
C	DATE	50 KHZ FILTER BANK (FRPF) BLOCK DIAGRAM AND SCHEMATIC
DRAWN BY K	DATE 4/1/80	
APPROVED BY JS	DATE 5/1/80	DRAWING NUMBER FRP-C-40 — SHEET 2 OF 2

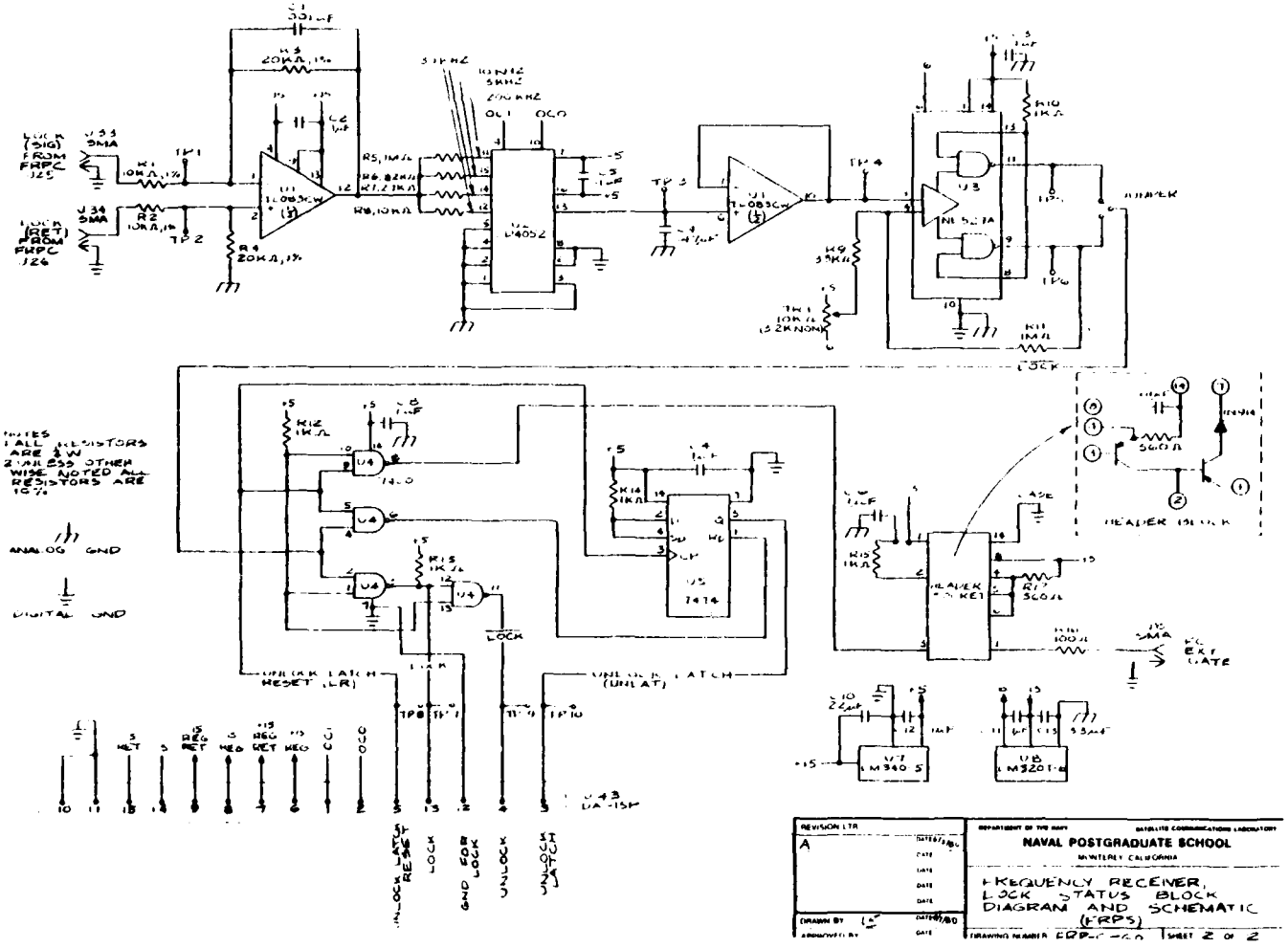


REVISION LTR	DEPARTMENT OF THE NAVY — NAVAL POSTGRADUATE SCHOOL, MONTEREY, CALIFORNIA
DRAWN BY: L S	FREQUENCY RECEIVER XT DRIVER BLOCK DIAGRAM AND SCHEMATIC (1 PPX)
APPROVED BY:	DRAWING NUMBER FRD C-50 SHEET 1 OF 2

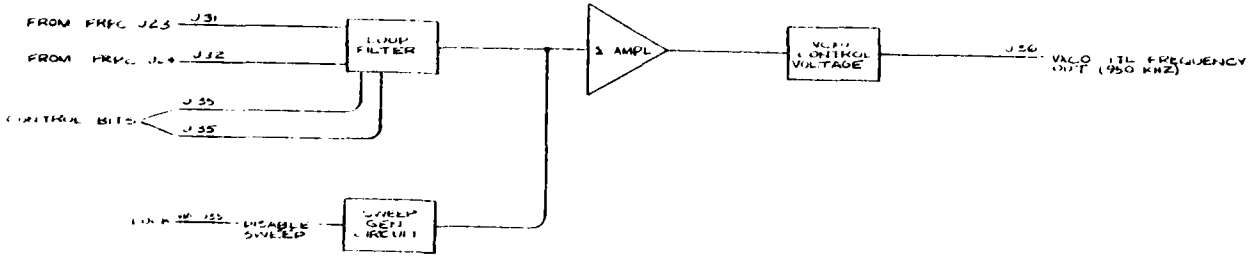

NAVAL POSTGRADUATE SCHOOL
FREQUENCY RECEIVER
DIGITAL GROUND
FLOAT LOAD GROUND
FROM FREQ VIA
CASE



REVISION LTR / DATE	DEPARTMENT OF THE NAVY — NAVAL POSTGRADUATE SCHOOL, MONTEREY, CALIFORNIA
DRAWN BY VF	FREQUENCY RECEIVER LOCK STATUS (FRPS) BLOCK DIAGRAM AND SCHEMATIC
APPROVED BY (PL), DATE	DRAWING NUMBER FRP L-61 SHEET 1 OF 2



REVISION LTR		DEPARTMENT OF THE NAVY — SATELLITE COMMUNICATIONS LABORATORY
A	DATE 7/80	NAVAL POSTGRADUATE SCHOOL
	DATE	MONTEREY, CALIFORNIA
	DATE	FREQUENCY RECEIVER, LOCK STATUS BLOCK DIAGRAM AND SCHEMATIC (FRPS)
	DATE	
DRAWN BY LF	DATE 7/80	
APPROVED BY	DATE	DRAWING NUMBER ERPS-[illegible]-00 SHEET 2 OF 2



REVISION / TR	DATE
	DATE
	DATE
	DATE
	DATE
DRAWN BY LS	DATE 4/84
APPROVED BY (1)+	DATE

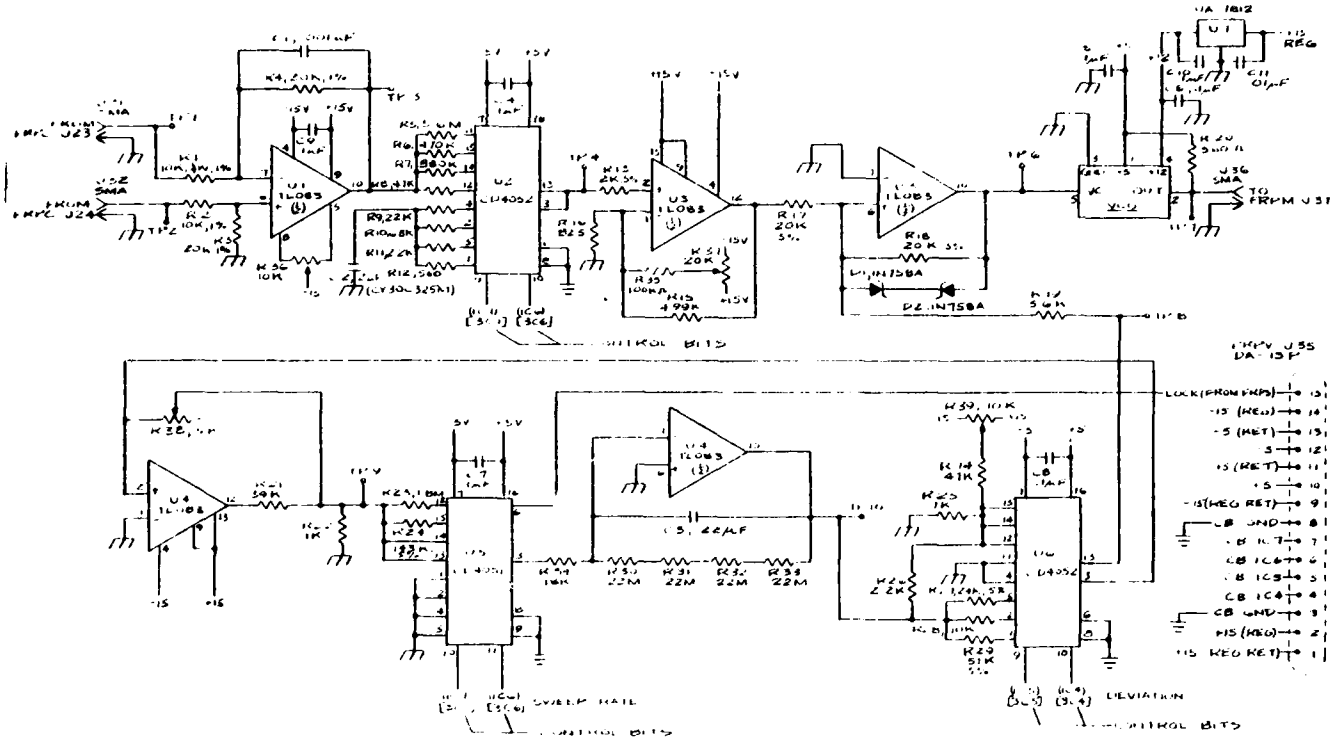
DEPARTMENT OF THE NAVY — SATELLITE COMMUNICATIONS LABORATORY

NAVAL POSTGRADUATE SCHOOL

MONTEREY, CALIFORNIA

FREQUENCY RECEIVER VCO MODULE BLOCK DIAGRAM AND SCHEMATIC (FRPV)

DRAWING NUMBER FRPV-1-TO | SHEET 1 OF 2



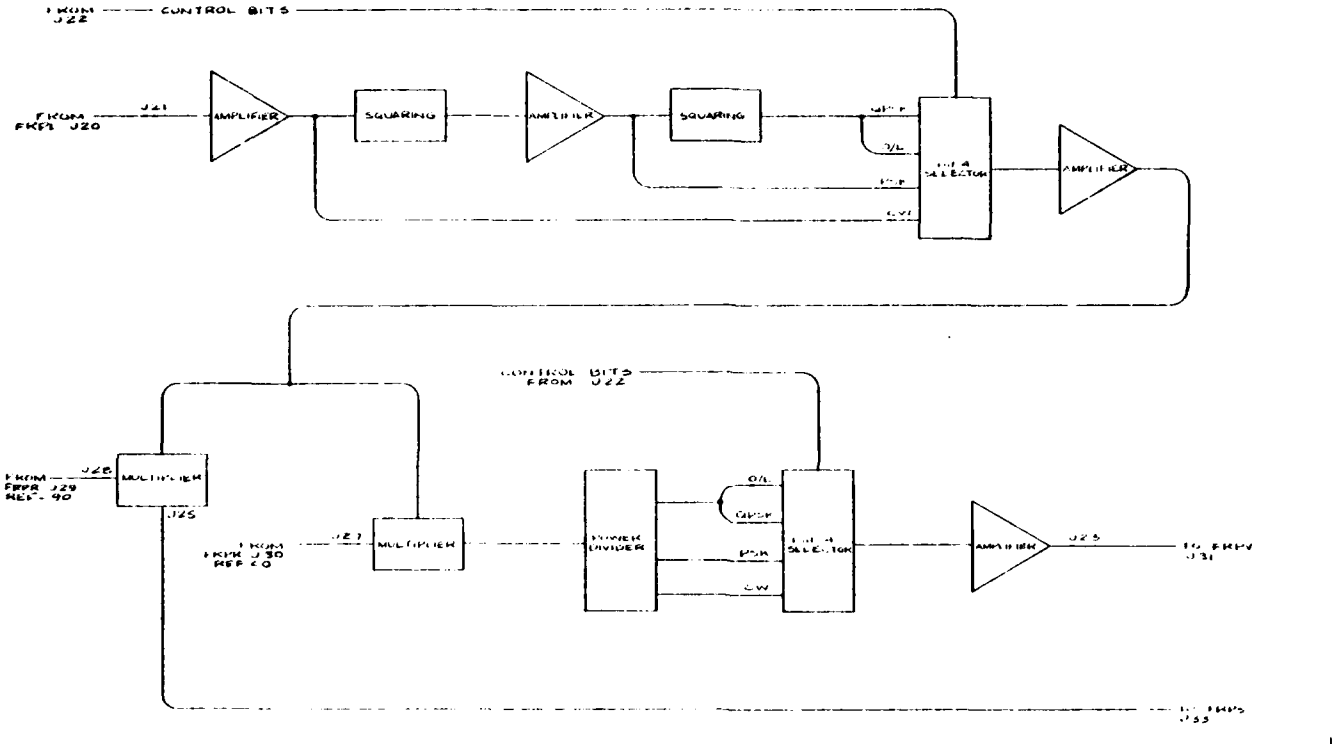
NOTES
1. ALL RESISTANCE VALUES ARE IN OHMS
2. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE ±1%
3. ( ) DENOTES USED ON FR 1
4. ( ) DENOTES USED ON FR 2

= ANALOG GROUND

= DIGITAL GROUND

5. CONNECTOR CONFIGURED FOR FR 1

REVISION LTR	DEPARTMENT OF THE NAVY — SATELLITE COMMUNICATIONS LABORATORY
A	NAVAL POSTGRADUATE SCHOOL MONTEREY CALIFORNIA
DRAWN BY	FREQUENCY RECEIVER VCO MODULE BLOCK DIAGRAM AND SCHEMATIC (FRPV)



REVISION LTR	DATE
	DATE
	DATE
	DATE
	DATE
DRAWN BY	DATE
APPROVED BY	DATE

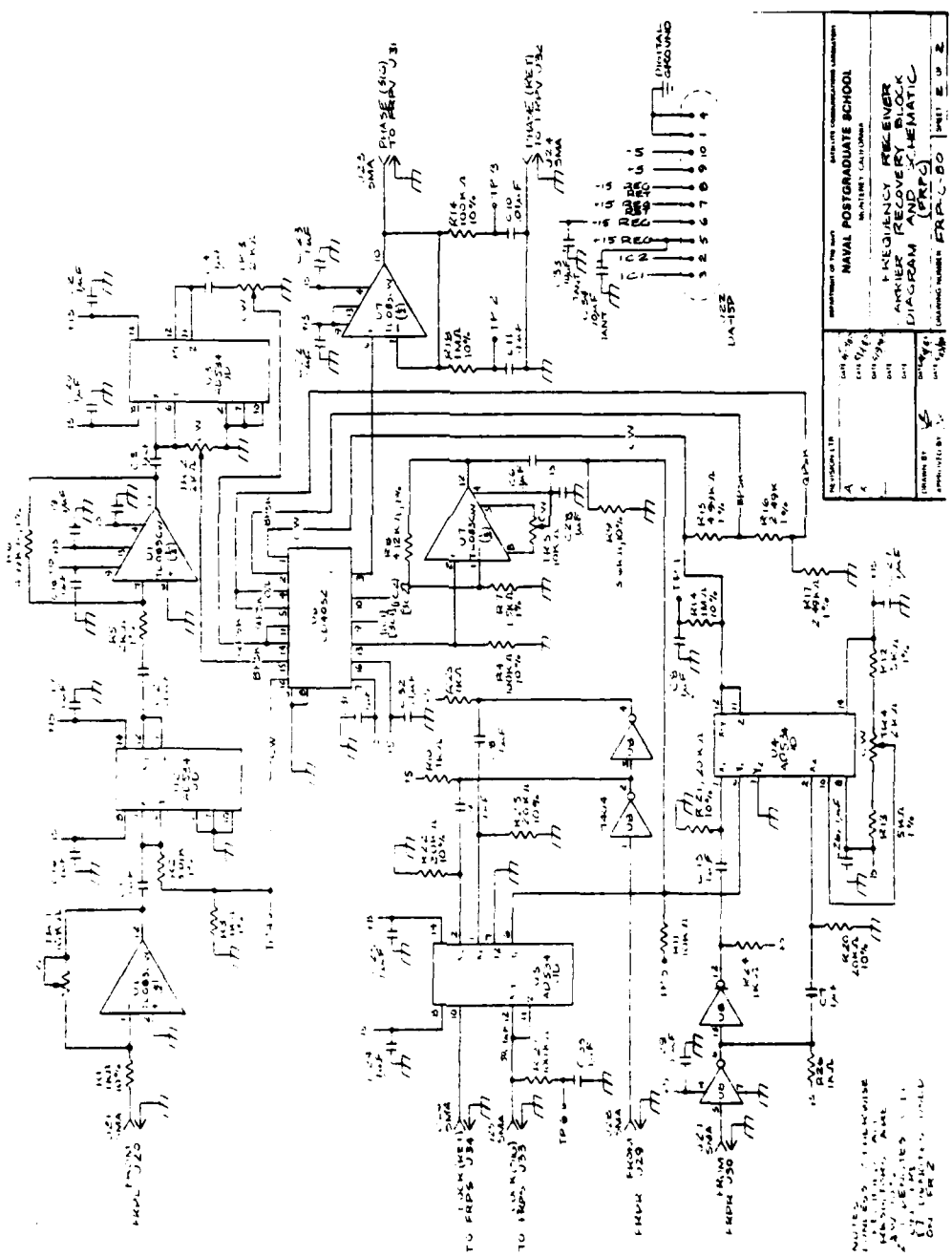
DEPARTMENT OF THE NAVY

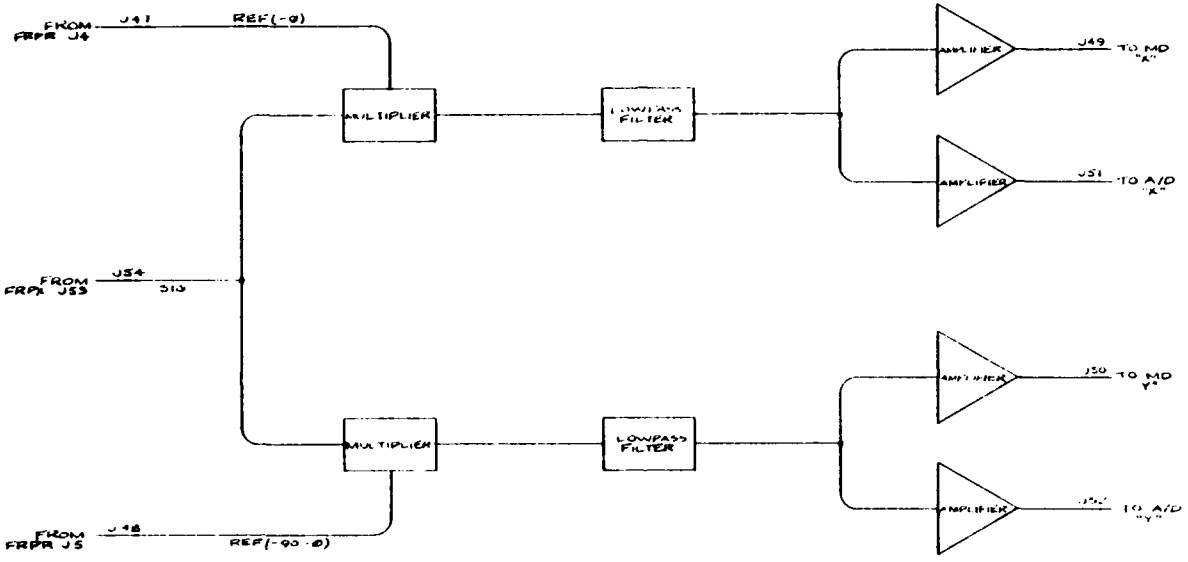
NAVAL POSTGRADUATE SCHOOL

MONTEREY, CALIFORNIA

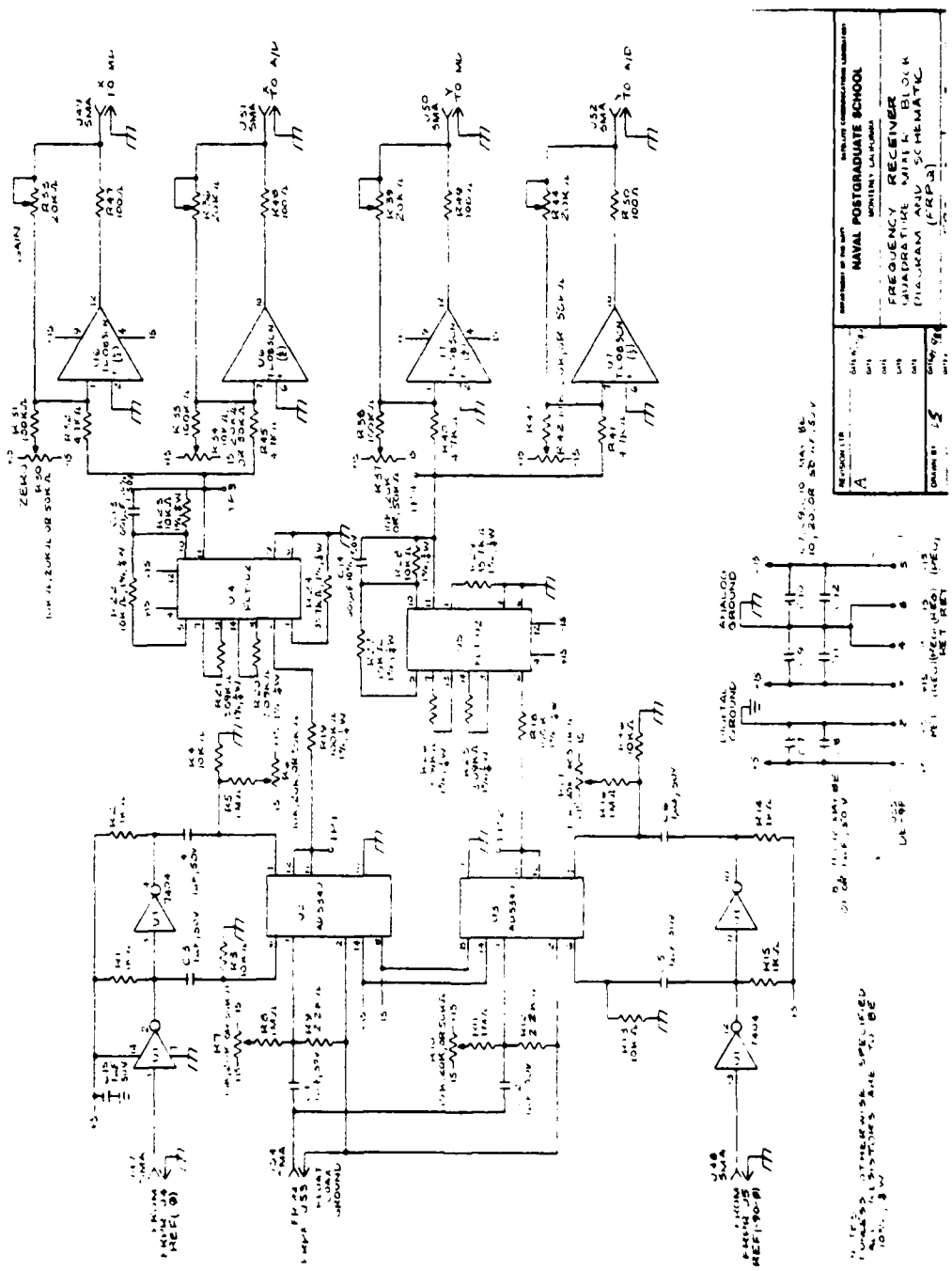
FREQUENCY RECEIVER CARRIER RECOVERY BLOCK DIAGRAM AND KINEMATICS

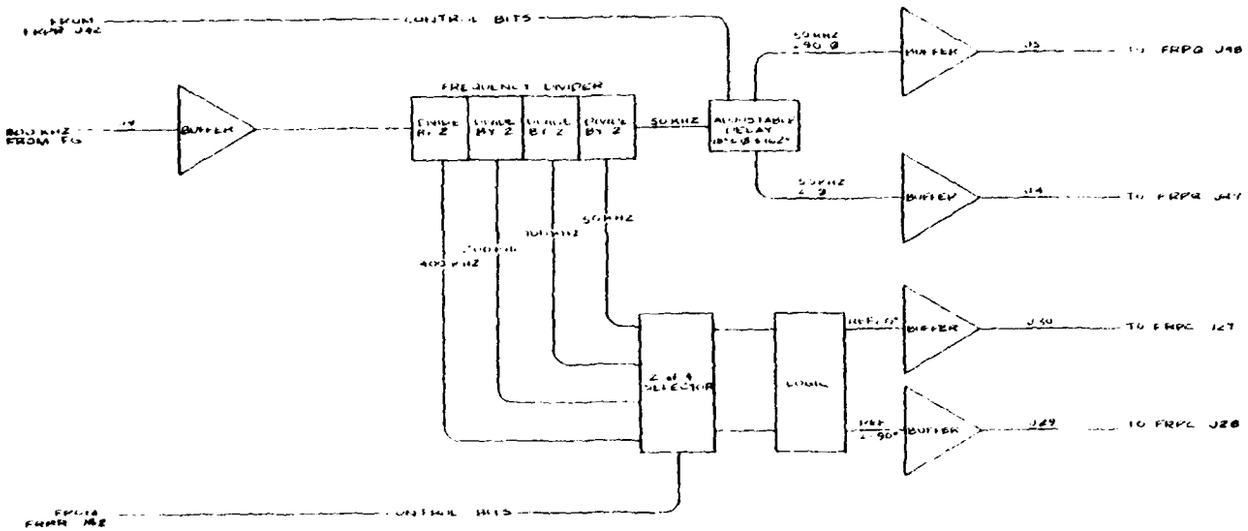
DRAWING NUMBER FREQ C 80 | SHEET 1 OF 2


NAVAL POSTGRADUATE SCHOOL
FREQUENCY RECEIVER
CARRIER RECOVERY BLOCK
DIAGRAM AND SCHEMATIC
(FRPC)
FRPC-80
DIGITAL GROUND

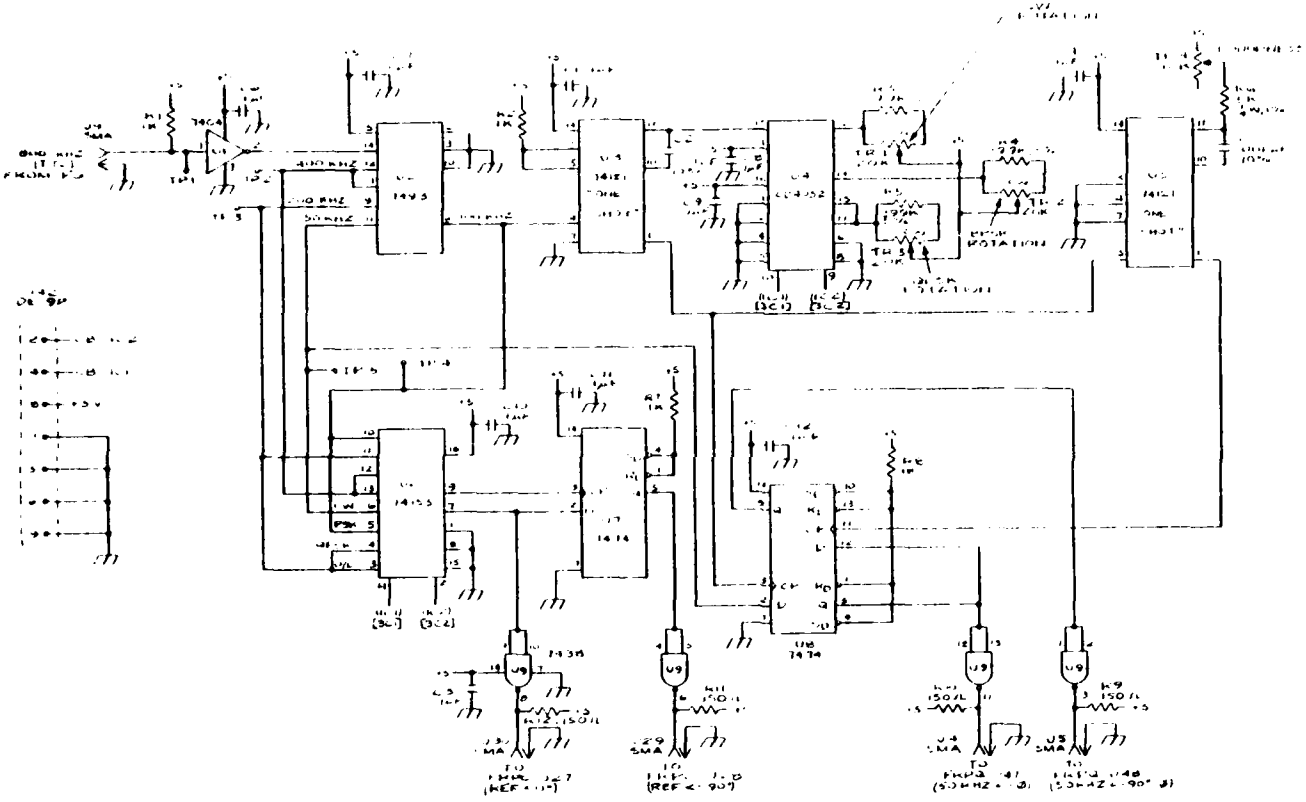


REVISION LTR	DEPARTMENT OF THE NAVY — SATELLITE COMMUNICATIONS LABORATORY **NAVAL POSTGRADUATE SCHOOL** MONTEREY CALIFORNIA
DATE	FREQUENCY RECEIVER QUADRATURE MIXER BLOCK DIAGRAM AND SCHEMATIC (FRPQ)
DRAWN BY	DRAWING NUMBER FRPQ-S1 — SHEET 1 OF 4
APPROVED BY	


NAVAL POSTGRADUATE SCHOOL
MONTEREY, CALIFORNIA
FREQUENCY RECEIVER
QUADRATURE MIXER BLOCK
DIAGRAM AND SCHEMATIC
(FRP2)
ANALOG GROUND
DIGITAL GROUND



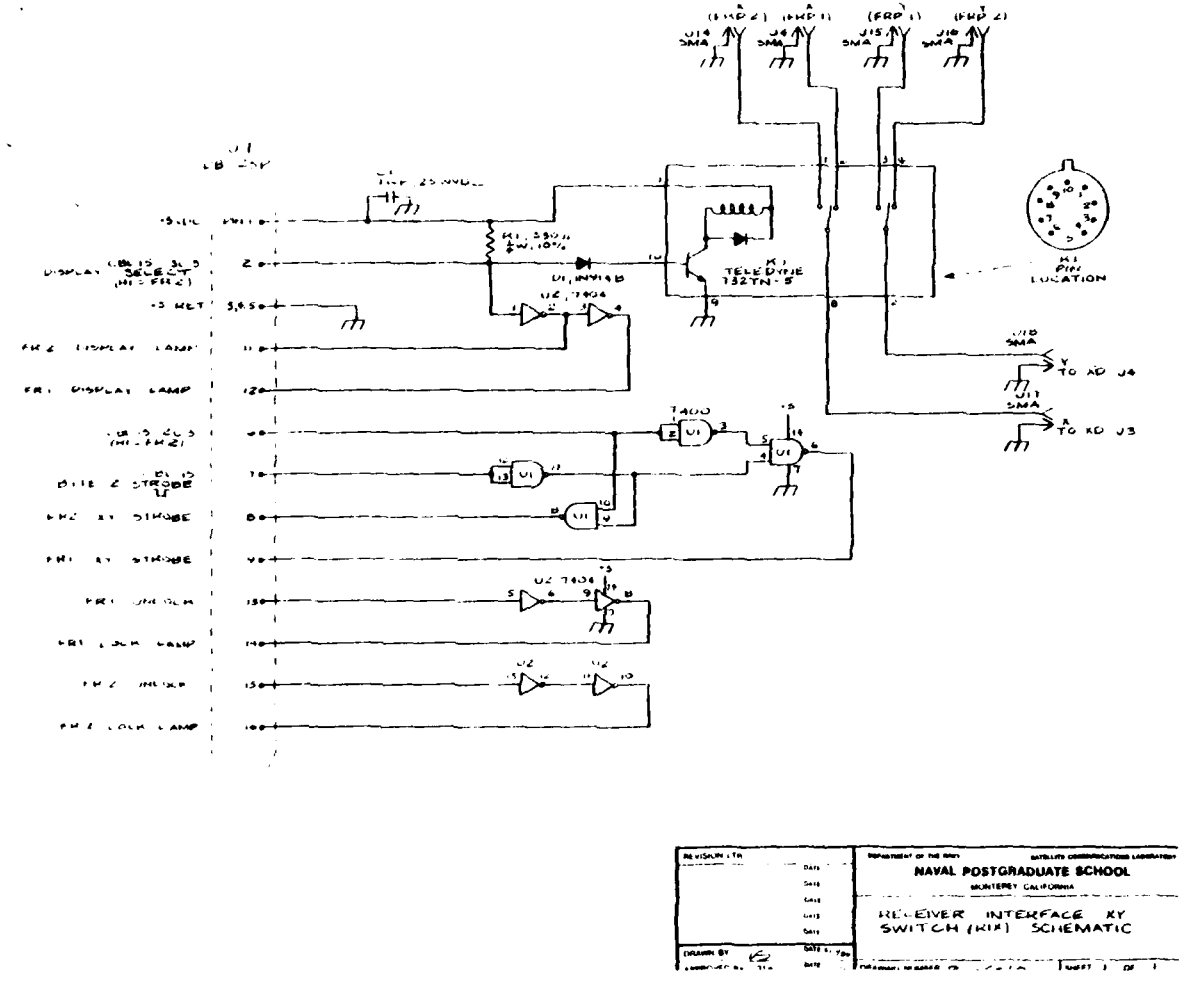
REVISION TR	NAVAL POSTGRADUATE SCHOOL MONTEREY CALIFORNIA
	FREQUENCY DIVIDER INTERNAL FREQUENCY GENERATOR BLOCK DIAGRAM AND SCHEMATIC (1 OF 7)



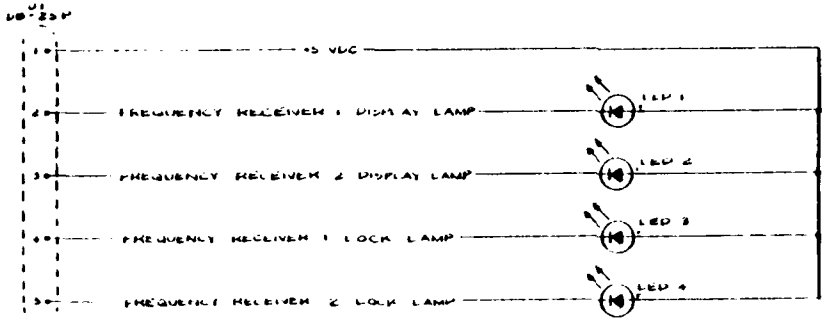
NOTES
1. ALL RESISTANCE VALUES ARE IN OHMS
2. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE ¼ W, 10%
3. C 2 AND C 3 ARE 10% TEMP STABLE
4. (S) INDICATES USED ON FR1
5. (L) INDICATES USED ON FR2

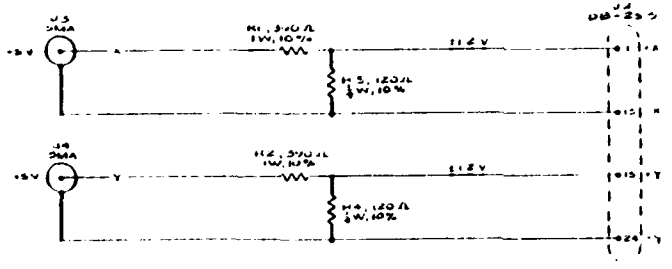
DIGITAL GROUND

REVISION LTR	NAVAL POSTGRADUATE SCHOOL
A	MONTEREY, CALIFORNIA
B	
C	FREQUENCY RECEIVER REFERENCE FREQUENCY GENERATOR BLOCK DIAGRAM AND SCHEMATIC (FRFR)
DRAWN BY	

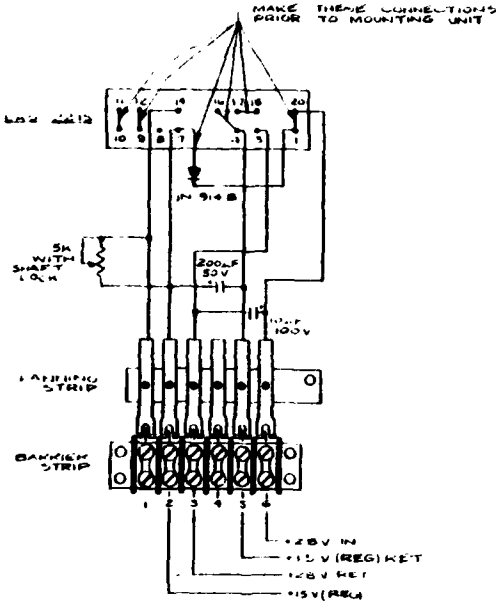


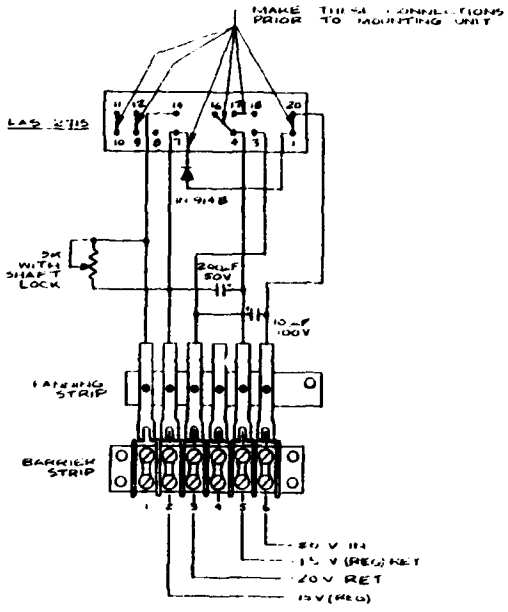
REVISION LTR	DEPARTMENT OF THE NAVY — SATELLITE COMMUNICATIONS LABORATORY **NAVAL POSTGRADUATE SCHOOL** MONTEREY CALIFORNIA
DRAWN BY	RECEIVER INTERFACE XY SWITCH (RIX) SCHEMATIC
APPROVED BY	DRAWING NUMBER — SHEET 1 OF 1



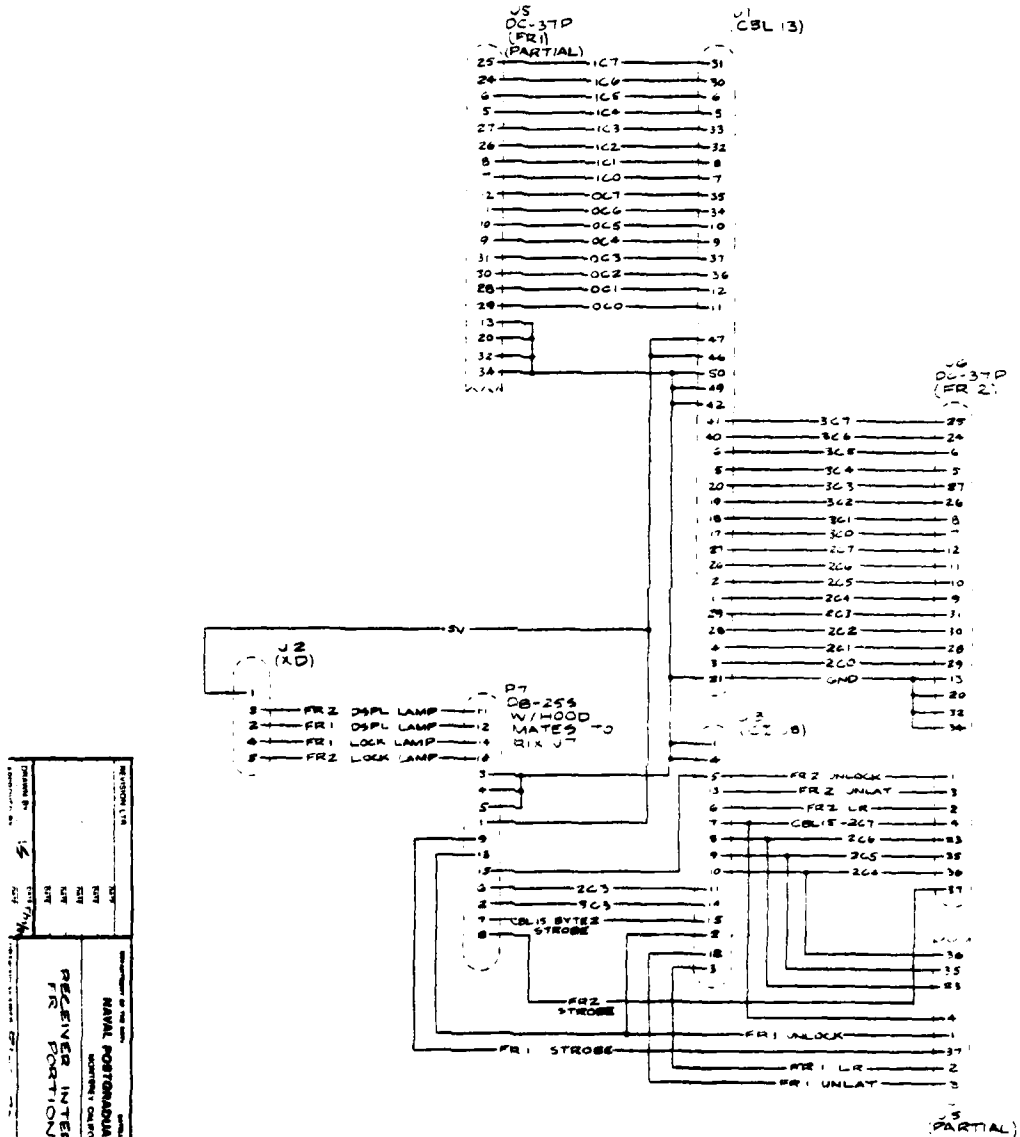


	NAVAL POSTGRADUATE SCHOOL MONTEREY CALIFORNIA
	11 DRIVER (RD) SCHEMATIC



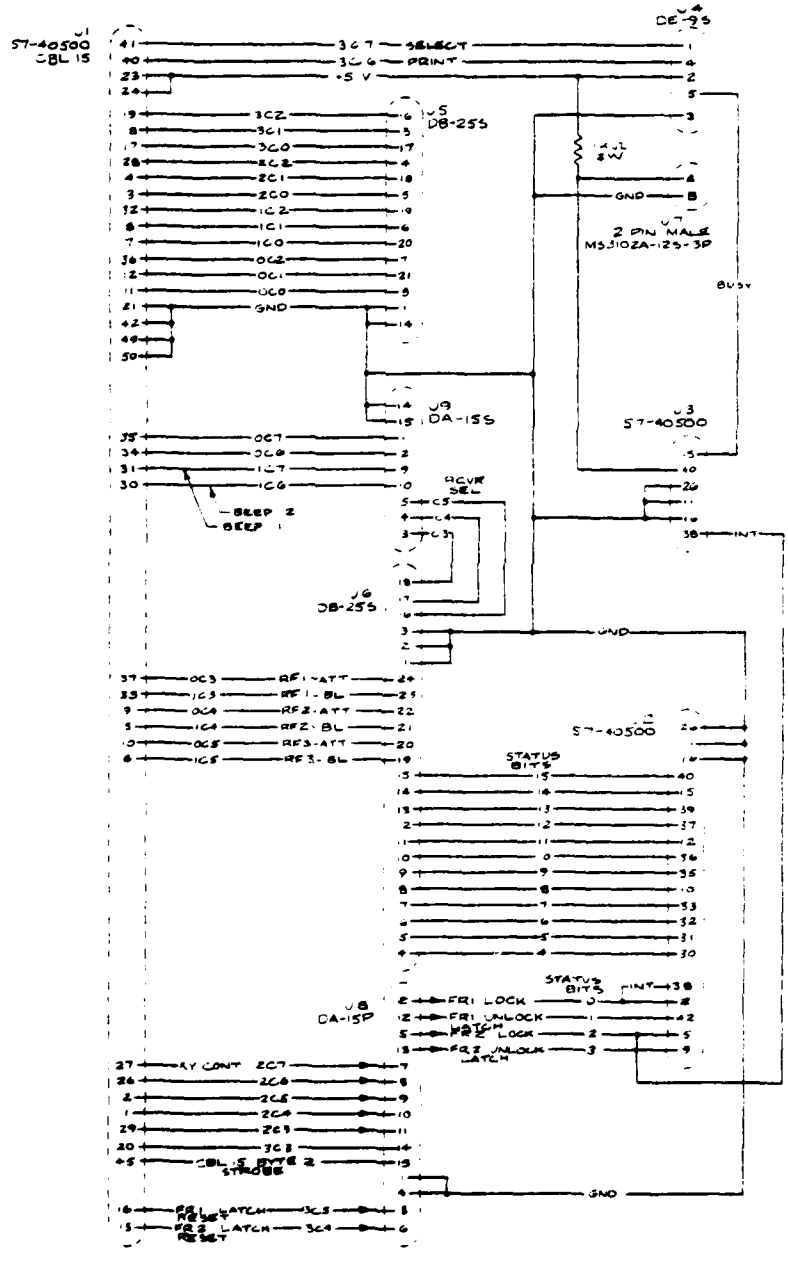


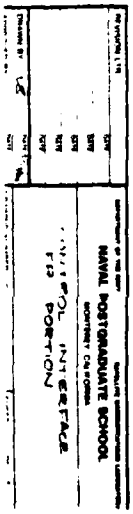
REVISION LTR		DEPARTMENT OF THE NAVY — SATELLITE COMMUNICATIONS LABORATORY
A	DATE	NAVAL POSTGRADUATE SCHOOL MONTEREY CALIFORNIA
	DATE	FREQUENCY RECEIVER POWER SUPPLY WIRING
DRAWN BY LS	DATE	DRAWING NUMBER FRP-C-07 SHEET 1 OF 1
APPROVED BY	DATE	



NAVAL POSTGRADUATE SCHOOL
MONTEREY, CALIFORNIA

RECEIVER INTERFACE
FR PORTION


S7-40500 CBL 15
SELECT
PRINT
+5 V
GND
DB-25S
DA-15S
DE-9S
2 PIN MALE MS3102A-12S-3P
S7-40500
RCVR SEL
BEEP 2
BEEP 1
INT
BUSY
RF1 ATT
RF1 BL
RF2 ATT
RF2 BL
RF3 ATT
RF3 BL
STATUS BITS
FR1 LOCK
FR1 UNLOCK
FR2 LOCK
FR2 UNLOCK
DA-15P
RY CONT
CBL 5 BYTE 2 STROBE
FR1 LATCH RESET
FR2 LATCH RESET


NAVAL POSTGRADUATE SCHOOL
INTERFACE
PORTION

APPENDIX B
PINOUTS FOR ASSEMBLIES

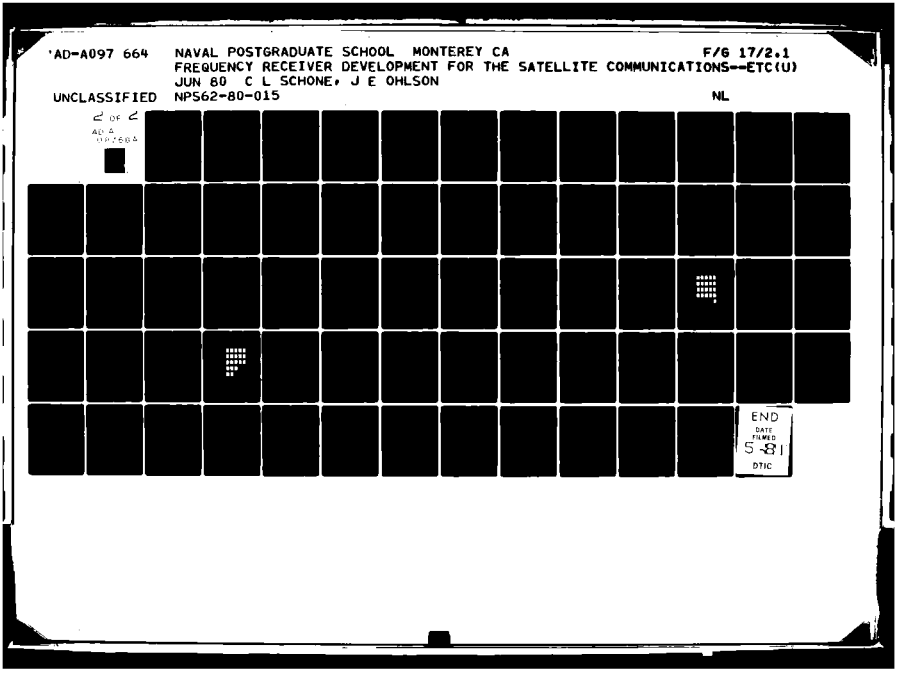
This appendix contains the multipin connector pinouts of all assemblies of the Frequency Receiver.

FREQUENCY RECEIVER PLUG PIN ASSIGNMENTS

FRP - FREQUENCY RECEIVER - PLL PANEL

MODULE	TYPE "D"	PIN #	SIGNAL
RI CONN. J3	37 - MALE	1	UNLOCK
		2	LATCH RESET
		3	UNLOCK LATCH
		4	2C7
		5	1C4
		6	1C5
		7	1C0
		8	1C1
		9	0C4
		10	0C5
		11	0C6
		12	0C7
		13	CONTROL BIT GROUND

		14-20	UNUSED
		20	CONTROL BIT GROUND
		21-22	UNUSED
		23	2C6
		24	1C6
		25	1C7
		26	1C2
		27	1C3
		28	0C1
		29	0C0
		30	0C2
		31	0C3
		32-34	UNUSED
		35	2C5
		36	2C4
		37	XY STROBE
FRPF	9 - MALE	1	+ 15 (REGULATED)
J18			
		2	CONTROL BIT GROUND
		3	0C0
		4	+ 5, - 5, - 15, + 15 (RETURN)
		5	-5
		6	- 15 (REGULATED)
		7	2C7 (DRIVEN FROM FRPX)
		8	0C1
		9	+5


AD-A097 664
NAVAL POSTGRADUATE SCHOOL MONTEREY CA
F/6 17/2.1
FREQUENCY RECEIVER DEVELOPMENT FOR THE SATELLITE COMMUNICATIONS--ETC(U)
JUN 80 C L SCHONE, J E OHLSON
UNCLASSIFIED
NPS62-80-015
NL
2 OF 2
AD A
097664
END
DATE FILMED
5-81
DTIC

FRPM	9 - MALE	1	CONTROL BIT GROUND
J40			
		2	+ 5
		3	
		4	+ 28
		5	CONTROL BIT GROUND & VOLTAGE RETURN
		6	DAICO CONTROL BIT
		7	1C0
		8	1C2
		9	1C1
FRPD	9 - MALE	1	CONTROL BIT GROUND
J44			
		2	1C2
		3	1C1
		4	UNUSED
		5	CONTROL BIT GROUND
		6	CONTROL BIT GROUND
		7	UNUSED
		8	+ 5
		9	CONTROL BIT GROUND
FRPR	9 - MALE	1	CONTROL BIT GROUND
J42			
		2	1C2
		3	
		4	1C1

		5	CONTROL BIT GROUND
		6	CONTROL BIT GROUND
		8	+ 5
		9	CONTROL BIT GROUND
FRPC	15 - MALE	1	CONTROL BIT GROUND
J22			
		2	1C2
		3	1C1
		4	CONTROL BIT GROUND
		5	+ 15 (REGULATED)
		6	- 15 (REGULATED)
		7	+ 15 (REGULATED)
		8	- 15 (REGULATED RETURN)
		9	+ 5
		10	- 5
		11-15	UNUSED
FRPV	15 - MALE	1	+ 15 (REGULATED RETURN)
J35			
		2	+ 15 (REGULATED)
		3	CONTROL BIT GROUND
		4	1C4
		5	1C5
		6	1C6
		7	1C7
		8	CONTROL BIT GROUND
		9	- 15 (REGULATED RETURN)

		10	+ 5
		11	+ 5 (RETURN)
		12	- 5
		13	- 5 (RETURN)
		14	- 15 (REGULATED)
		15	LOCK (FROM FRPS)
FRPQ	9 - MALE	1	+5
J55			
		2	+ 5 (RETURN)
		3	+ 15 (REGULATED)
		4	+ 15 (REGULATED RETURN)
		5	- 15 (REGULATED)
		6	- 15 (REGULATED RETURN)
		7-9	UNUSED
FRPS	15 - MALE	1	0C1
J43			
		2	0C0
		3	UNLOCK LATCH
		4	UNLOCK
		5	LATCH RESET
		6	+ 15 (REGULATED)
		7	+ 15 (REGULATED RETURN)
		8	- 15 (REGULATED)
		9	- 15 (REGULATED RETURN)
		10	CONTROL BIT GROUND
		11	CONTROL BIT GROUND

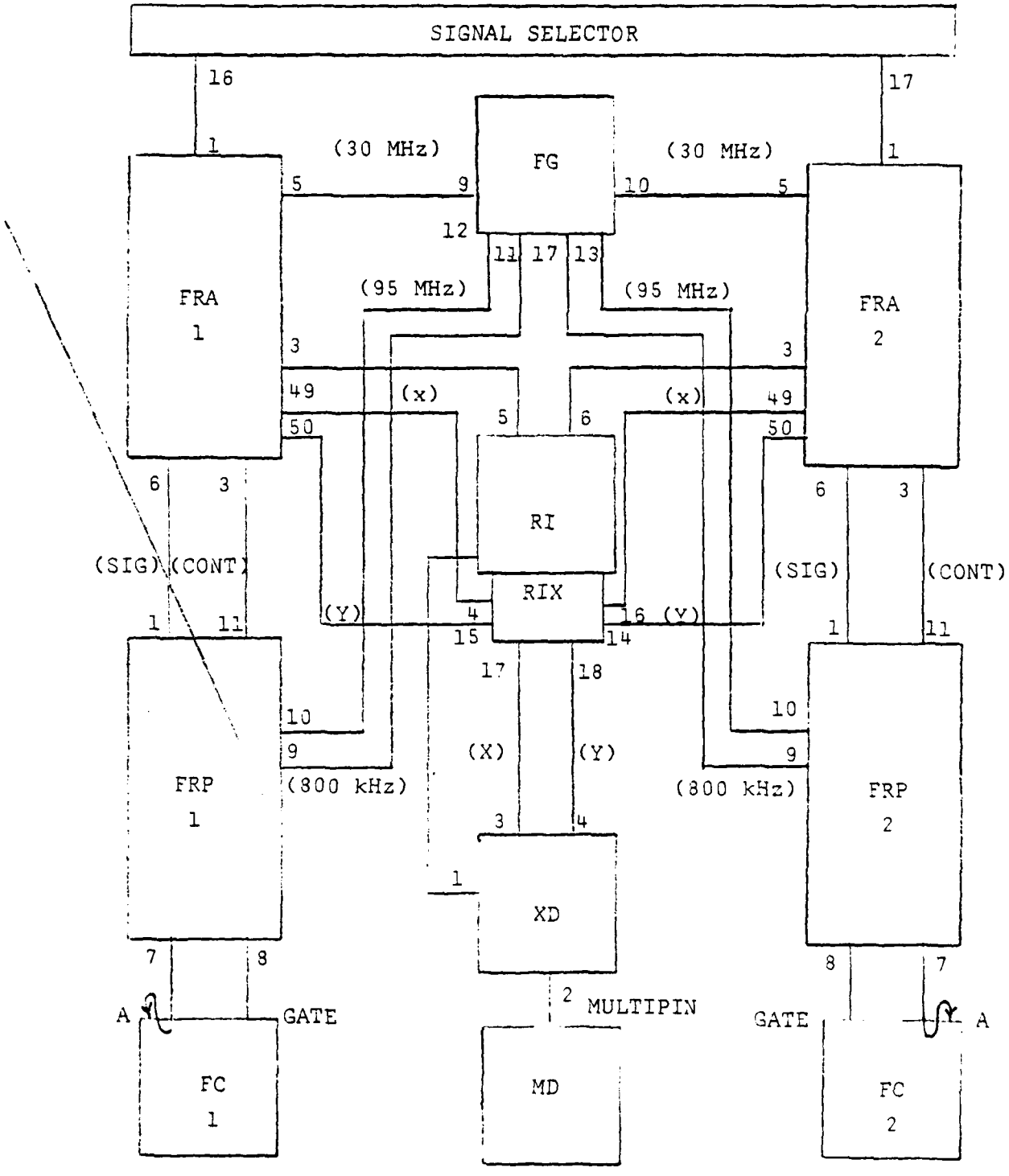
		12	LOCK GROUND
		13	LOCK
		14	- 5
		15	- 5 (RETURN)
FRA	15 - MALE	1	DAICO CONTROL BIT
(DRIVEN)			
J11			
		2	0C6
		3	0C5
		4	0C4
		5	0C7
		6	0C3
		7	0C2
		8	CONTROL BIT GROUND
		9	CONTROL BIT GROUND
		10-15	UNUSED
FRPX	25 - MALE	1	+ 15 (REGULATOR)
J45			
		2	2C7 (DRIVEN TO FRPF)
		3	+ 15 (REGULATED RETURN)
		4	- 15 (REGULATED RETURN)
		5	-5
		6	- 15 (REGULATED)
		7	- 5 (RETURN)
		8	XY STROBE
		9	+ 5

10	+ 5 (RETURN)
11	CONTROL BIT GROUND
12	2C4
13	2C5
14	2C6
15	2C7
16-25	UNUSED

APPENDIX C

CABLING

This appendix contains a diagram which shows the Frequency Receiver coaxial and multipin cabling.


SIGNAL SELECTOR
16
17
1
(30 MHz)
FG
(30 MHz)
1
5
9
10
5
12
11
17
13
(95 MHz)
(95 MHz)
FRA
1
FRA
2
3
3
49
(x)
(x)
49
5
6
50
50
6
3
6
3
RI
(SIG)
(CONT)
(SIG)
(CONT)
RIX
(Y)
4
16
(Y)
1
11
15
14
1
11
17
18
10
10
9
(X)
(Y)
9
(800 kHz)
(800 kHz)
FRP
1
FRP
2
3
4
1
XD
7
8
8
7
2
MULTIPIN
A
GATE
GATE
A
FC
1
MD
FC
2

APPENDIX D
ASSEMBLY PARTS LIST

This appendix contains a parts list of components for the Frequency Receivers.

FRA PARTS LIST

MIXERS

FRAM1,M2 - MERRIMAC DMM - 4250

AMPLIFIERS

A1 - ANZAC, AM - 105

A2 - ANZAC, AM - 102

A3,4 - ANZAC, AM - 108

A5 - ANZAC, AM - 110

FILTERS

F1 - K & L, TUBULAR, 4B340-29/1-0

F2 - TYCO CRYSTAL FILTER, 001-34-760

F3 - K & L 4B50-29/2.5-0

F4 - K & L, 2B50-1/0.2-0

ATTENUATORS

AT1,4 - ELCOM, 3 DB, AT-50-3

AT2 - DAICO STEP ATTENUATOR 100C 1428-1D

AT3 - DAICO STEP ATTENUATOR 100D0589-6-A-.5,1,2,4,8,32

AT5 - VARIABLE ATTENUATOR MERRIMAC ARM - 1

FRP STAND ALONE PARTS LIST

MIXER

FRPMX - MINICIRCUITS LABS, ZFM-3H

FILTER

FRPFL - K & L, LOW PASS FILTER, 3L53-0.1-0

HARDWARE

Panel quantities are per each receiver to be constructed.

1 ALODYNED 8 3/4" x 19" PANEL (FRP)

1 " 8" x 19" PANEL (FRP)

1 " 5 1/4" x 19" PANEL (FRA)

MISC. STANDOFFS AND NUTS

FRPF PARTS LIST

RESISTORS

R1, R2 = 560 OHM, 1/4 WATT, 10 %

R3 = 56 " " "

R4, R5 = 1 KOHM, " "

R6, R7 = 2.2 " " "

R8, R9 = 1 " " "

R11 = 2 " " 1 %

R12 = 32.4 " " "

R13 = 100 " " 10 %

R14 = 220 " " "

R15 = 5.6 " " "

R16 = 100 " " "

R17 = 1 " " "

R18 = 2.7 " " 5 %

R19 = 4.99 " " 1 %

R20 = 49.9 " " "

R21 = 4.99 " " "

CAPACITORS

C1 - C13 = C15 = C18 = 0.1 uF, CERAMIC, 35 PV MIN.

C14 = C16 = C17 = 10 uF, CERAMIC, 35 PV MIN.

POTENTIOMETERS

TR1,2,3 = 5 KOHM BOURNE RJ26FW502

TR4 = 1 KOHM BOURNE RJ26FW102

DIODES

D1 = D2 = 1N914

RELAY

K1 = TELEDYNE 732TN-5

FILTERS

F1 = TTE BPF K1426, BW = 3 kHz AT 50 kHz

F2 = TTE BPF K1427, BW = 10 kHz AT 50 kHz

F3 = COMSTRON (WALL THICKNESS =0.12 ") SEG. FA 2594, BW = 200 HZ AT 50 kHz

HARDWARE

5 SMA-F BULKHEAD

1 DA -1tP CONNECTOR

1 BOX - COMPAC 5123-175-1 (6" x 3" x 1 3/4 ")

INTEGRATED CIRCUITS

U1 = 7400

U2, U6 = CD4052

U3, U4, U5 = TL083C

FRPL PARTS LIST

RESISTORS

R1 - 51 OHM, 1/4 WATT, 10 %

R2 - 2.2 K OHM, " "

R3 - 68 K OHM, 1/4 WATT, 10 %

R4 - 33 K OHM, " "

R5 - 1 K OHM, " "

R6 -100 K OHM, " 1 %

R7 -35.7 K OHM, " 1 %

R8 - 604 OHM, " 1 %

R9 - 604 OHM, " 1 %

R10 - 2.5 K OHM, " 1 %

R11 - 6.04 K OHM, 1/4 WATT, 1 %

CAPACITORS

C1, C2 - 10 PF, 35 WVDC MIN CERAMIC

C3,4,6-10 - 0.1 uF, 35 WVDC MIN, CERAMIC

C5 - 500 PF, 35 WVDC MIN, CERAMIC

C11,12 - 1.0 uF, 35 WVDC MIN, CERAMIC

C13,14 - 0.001 uF, 35 WVDC MIN, FEEDTHROUGH

INTEGRATED CIRCUITS

U1 - TL083C

U2 - DATEL FLT-U2 ACTIVE FILTER

DIODES

D1,2,3,4 - 1N914

HARDWARE

2 SMA-F

1 BOX - COMSTRON (WALL THICKNESS =0.12 ") 5117-175-1 (3" x 2" x 1 3/4")

FRPC PARTS LIST

RESISTORS

All resistors 1/4 watt, 10 % unless noted.

R1,10,11,24,25,26 - 1K OHM

R2 - 3.01 K OHM, 1 %

R4,19 - 100 K OHM

R5 - 2 K OHM, 1 %

R6,15 - 4.99 K OHM, 1 %

R7 - 1.5 K OHM, 1 %

R8 - 4.12 K OHM, 1 %

R9 - 5.6 K OHM

R12,13 - 5 K OHM, 1 %

R14,18 - 1 M OHM

R16,17 - 2.49 K OHM, 1 %

R19 - 100 K OHM, 1 %

R20,21,22,23 - 20 K OHM

POTENTIOMETERS

TR1,5 - 10 K OHM BOURNE

RT2,3,4 - 2 K OHM BOURNE

CAPACITORS

C1-C9 - 0.1 uF 16 WVDC min., CERAMIC

C10 - 0.01 uF, 16 WVDC MIN, CERAMIC

INTEGRATED CIRCUITS

U1,7 - TL083C

U2-5 - AD534JD

U6 - CD4052

U8 - 7404

HARDWARE

7 SMA-F BULKHEAD

1 DA-15P CONNECTOR

1 BOX, COMPAC (WALL THICKNESS = 0.12") 5123-175-1 (6" x 3" x

1 3/4")

FRPV PARTS LIST

RESISTORS

All resistors 1/4 watt, 10 % unless otherwise noted.

R1,2 - 10 K OHM, 1 %

R3,4 - 20 K OHM, 1 %

R5 - 5.6 M

R6 - 470 K OHM

R7 - 56 K OHM

R8 - 4.7 K OHM

R9 - 22 K OHM

R10 - 6.8 K OHM

R11,26 - 2.2 K OHM

R12,20 - 560 OHM

R13 - 2 K OHM, 5 %

R14 - 47 K OHM

R15 4.99 K OHM, 1 %

R16 825 OHM, 1 %

R17,18 - 20 K OHM, 5 %

R19 - 5.6 K OHM

R21 - 39 K OHM

R22,25 - 1 K OHM

R23 - 1.8 M OHM

R24 - 147 K OHM, 5 %

R27 - 25 K OHM

R28 - 10 K OHM

R29 - 51 K OHM, 5 %

R30,31,32,33 - 22 M OHM

R34 - 18 K OHM

R35 - 100 K OHM

R36,39 - 10 K OHM BOURNE POT

R37 - 20 K OHM BOURNE POT

R38 - 5 K OHM BOURNE POT

CAPACITORS

C1 - 0.001 uF, 16 WVDC MIN, CERAMIC

C2 - 2.0 uF, CY30C325M

C3 - 0.22 uF, 16 WVDC MIN.

C4-8,10 - 0.1 uF, 16 WVDC MIN, CERAMIC

C11 - 0.01 uF, 16 WVDC MIN, CERAMIC

DIODES

D1,2 - 1N758A 10 V ZENNER

INTEGRATED CIRCUITS

U1,3,4 - TL083C

U2,6 - CD4052

U5 - CD4051

U7 - -A 7812 (12 V REG)

OSCILLATOR

VCO - MONITOR 7124-01 VCXO 95 kHz CONTROL VOLTAGE = +/- 10 VDC

HARDWARE

3 SMA-F BULKHEAD

1 DA-15P CONNECTOR

1 BOX COMPAC (WALL THICKNESS = 0.22") SPECIAL NO PART NO. (7" x 8" x 1 3/4")(OUTSIDE)

FRPM PARTS LIST

RESISTORS

All resistors are 1/4 watt, 10 % unless specified otherwise.

R1,3 - 1 K OHM

R2 - 150 OHM, 1/2 WATT

R4,5 - 68 OHM, 1 WATT

CAPACITORS

C1-5 - 0.1 uF, 35 WVDC MIN, CERAMIC

C4 - 500 pF, 16 WVDC MIN, CERAMIC

INTEGRATED CIRCUITS

U1 - 74153

U2,3 - 7438

U4 - 7404

U5 - ULN2003A

TRANSFORMER

T1 - T1-1 RF Transformer (Mini-circuits)

HARDWARE

4 SMA-F BULKHEAD

1 DE-9P CONNECTOR

1 BOX - COMPAC (WALL THICKNESS = 0.12") 5120-175-1 (6" x 2" x 1 3/4")

FRPD PARTS LIST

RESISTOR

R1 - 100 K OHM, 1/4 WATT, 10 %

CAPACITORS

C1-4 - 0.01 uF, 50 WVDC MIN, CERAMIC

INTEGRATED CIRCUITS

U1 - SP8629 (PLESSEY)

U2 - 74H10

HARDWARE

2 SMA-F BULKHEAD

1 DE-9P CONNECTOR

1 BOX - COMPAC (WALL THICKNESS = 0.12") 5117-175-(3" x 2"

x 1 3/4")

FRPS PARTS LIST

RESISTORS

All resistors 1/4 watt, 10 % unless otherwise noted.

R1,2 - 10 K OHM, 1 %

R3,4 - 20 K OHM, 1 %

R5,11 - 1 M OHM

R6 - 82 K OHM

R7 - 27 K OHM

R8 - 10 K OHM

R9 - 33 K OHM

R10,12,13,14,15 - 1 K OHM

R17 - 560 OHMS

R16 - 100 OHMS

POTENTIOMETERS

TR1 - 10 K OHM BOURNE

CAPACITORS

C1 - 0.001 uF, 16 WVDC MIN, CERAMIC

C2,3,5,6,8,11,12 - 0.1 uF, 16 WVDC MIN, CERAMIC

C7 - 0.01 uF, 16 WVDC MIN. CERAMIC

C4 - 0.47 uF, 16 WVDC MIN. CERAMIC

C10 - 0.22 uF, 30 WVDC MIN, TANT

C13 - 0.33 uF, 30 WVDC MIN, TANT.

INTEGRATED CIRCUITS

U1 - TL083C

U2 - CD4052

U3 - NE 527

U4 - 7400

U5 - 7474

U6 - MC10124

U7 - LM 340-5

U8 - LM 320T-6

HARDWARE

3 SMA-F BULKHEAD

1 DA - 15P CONNECTOR

1 BOX - COMPAC (WALL THICKNESS = 0.12") 5123-175-1 (6" x 3" x 1 3/4")

FRPX PARTS LIST

RESISTORS

All resistors are 1/4 watt, 10 % unless otherwise specified.

R1,2,4 - 3.01 K OHM, 1 %

R5,6,9,14 - 10 K OHM, 1 %

R7 - 2.49 K OHM, 1 %

R8 - 4.99 K OHM, 1 %

R10,15 - 20 K OHM in parallel with 169 K OHM, 1 %

R11,16 - 32 K OHM in parallel with 1 M OHM, 1 %

R12,17 - 49.9 K OHM in series with 6.04, 1 %

R13 - 100 K OHM, 1 %

R18 - 1 K OHM

R19 - 470 K OHM

CAPACITORS

C1,2,3,12-20 - 0.1 uF, 35 WVDC MIN., CERAMIC

C4-7 - 0.01 uF, 35 WVDC, MIN.. CERAMIC

C8-11 - 10.0 uF, 35 WVDC MIN, TANT.

INTEGRATED CIRCUITS

U1,2 - TL083CN

U3,4 - CD4051

U5 - 74175

HARDWARE

2 SMA-F BULKHEAD

1 DB - 25P CONNECTOR

1 BOX - COMPAC (WALL THICKNESS = 0.12") 5123-175-1 (6" x 3" x 1 3/4")

FRPR PARTS LIST .

RESISTORS

All resistors 1/4 watt, 10 % unless noted otherwise.

R1,27,8 - 1 K OHM

R3,4,5 - 39.9 K OHM, 5 %

R6 - 5 K OHM, 1 %

R9-12 - 150 OHM

POTENTIOMETERS

TR1,2,3 - 20 K OHM BOURNE

TR4 - 10 K OHM BOURNE

CAPACITORS

C1,4,5 - 0.1 uF, 35 WVDC MIN, CERAMIC

C2,3 - 0,001 uF, 35 WVDC, 10 % TEMPERATURE STABLE.

INTEGRATED CIRCUITS

U1 - 7404

U2 - 7493

U3,5 - 74121

U4 - CD4052

U6 - 74153

U7,8 - 7474

U9 - 7438

HARDWARE

5 SMA-F BULKHEAD

1 DE-9D

1 BOX - COMPAC (WALL THICKNESS = 0.12") 5120-175-1 (6" x 2" x 1 3/4")

RIK PARTS LIST

RESISTORS

All resistors are 1/4 watt, 10 % unless otherwise specified.

R1 - 680 OHM

R2 - 330 OHM RELAY

K1 - TELEDYNE 732TN-5

CAPACITOR

C1 - 0.1 uF, 25 WVDC MIN., CERAMIC

INTEGRATED CIRCUITS

U1 - 7400

U2 - 7404

HARDWARE

6 SMA-F BULKHEAD

1 DB - 25P CONNECTOR

1 BOX - COMPAC (WALL THICKNESS = 0.12") 5117-175-1 (3" x 2" x 1 3/4")

XD PARTS LIST

RESISTORS

All resistors 1 watt, 10 %.

R1,2 - 390 OHMS

R3,4 - 120 OHMS

LED'S

4 DIALIGHT 249-7968-3732-50, LED, RED 5 V.

HARDWARE

2 SMA-F BULKHEAD

1 DB - 25P CONNECTOR

APPENDIX E
TESTING/ALIGNMENT PROCEDURES

FREQUENCY RECEIVER ALIGNMENT PROCEDURES

NOTE:

Control bit senses are negative logic unless otherwise specified. Notation used here is H = high = voltage present = switch in NAVPGSCOL "bit box" is in down position when box configured for negative logic. Also L = low = no voltage = switch in "bit box" in up position when configured for negative logic. Positive logic is configured in the opposite voltage sense. Test frequency and open loop frequency are to be coherent, i.e., on the SSA frequency standard.

1. Establish alignment presets:

a. FRA 32 dB attenuators in the nonattenuating position; i.e., CBL13-100 = OC7 = H.

b. FRA IF attenuation is 5 dB; CBL13 - OC6 = OC4 = OC2 = H and OC5 = OC3 = L.

c. Frequency Receiver is in OPEN LOOP; CBL13 - 102 = 101 = H.

d. Set up test frequency of 30 MHz at a level determined by the insertion point chosen in step two below.

e. Select the 30 kHz IF filter; i.e., CBL13 - OC1 = OC0 = L.

2. Inject the test signal:

This is accomplished in one of two different means dependent

upon wheather the SSA system is in a position to support the calibration method:

a. If the SSA can directly provide the test signal then it will be inserted into the SSU at -55 dBm. The LO in support of the receiver in calibration will be automatically set to the correct frequency if the computer is told to configure the receiver for a received frequency of 260.00 MHz.

b. If direct injection is required, the test signal may be inserted into the front end of FRA (J1) at a -66 dBm level. Here also the LO must be set. This may be accomplished either in the above manner, or directly setting the supporting LO to 109.00 MHz.

3. Adjust the ARM-1 (AT-5) for a -3.6 dBm 50 kHz signal at the output of FRPFL into 50 ohms.

4. Selecting each of the IF bandwidths in turn, adjust their gains for an output level of 1.12 VRMS (1.6 V Peak). This is accomplished by selecting the 30 kHz filter with OC0 = OC1 = L on CBL13-and adjusting potentiometer TR3. The 10 kHz filter is selected by setting OC1 = L and OC0 = H and adjusting potentiometer TR2. The 3 kHz width is set by setting OC1 = H and OC0 = L and adjusting potentiometer TR1. Finally the 0.2 kHz width is set by selecting OC1 = OC0 = H and adjusting potentiometer TR4. The accuracy of this adjustment may be confirmed by comparing displays on the MD. Equivalent gains will result in displays which are of equivalent distances from the center of the display.

5. Perform the following checks/adjustments on FRPR to set the reference frequencies:

a. Examine test points one thru five and establish the presence of the following signals:

TP1 - 800 kHz TTL (PERIOD = 1.25 uSEC)

TP2 - 400 kHz TTL (PERIOD = 2.5 uSEC)

TP3 - 200 kHz TTL (PERIOD = 5.0 uSEC)

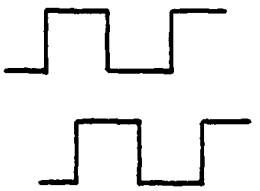
TP4 - 100 kHz TTL (PERIOD = 10.0 uSEC)

TP5 - 50 kHz TTL (PERIOD = 20.0 uSEC)

b. Select the following modes and ensure the following:

1C1	1C2	MODE	J29	J30
L	L	CW	50 kHz angle 90	50 kHz angle 0
L	H	BPSK	200 kHz angle 90	200 KHS angle 0
H	L	QPSK	100 kHz angle 90	100 kHz angle 0
H	H	QPSK	100 kHz angle 90	100 kHz angle 0

Ninetydegree difference of waveforms is equivalent to:



c. Observe J4 and J5 and ensure that this output remains 50 kHz at 90 degrees for all the above states.

d. Select OPEN LOOP i.e. 1C1 = 1C0 = H, and observing at J4 and J5 adjust TR4 if the above waveform is not at 90 degrees.

6. Validate that the output of FRPL is of the order of 1.5 V peak. If not then one or all of the diodes D1 - D4, or operational amplifier U1, or the power supply is faulty.

7. Perform the following OPEN LOOP MODULATION DISPLAY alignment:

a. Set CBL15-2C7 = 2C6 = 2C5 = 2C4 = L. This sets the FRPF to FRPX voltage gain to 7.5 and the FRPX voltage gain to 2.

b. With an OPEN LOOP offset of approximately 50 Hz, adjust R33 to give a 0.68 V peak signal on FRPQ J49, and R39 for a similar value at J50.

c. R30 and R37 may be adjusted to give a centered display or equivalently a slowly varying sinusoid about zero dc.

d. For small imbalances in XY dispaly which give an oblong MD display in OPEN LOOP, trim only the Y axis potentiometer (R39) in FRPQ.

e. Note that the MD must be independently calibrated via its internal potentiometers so that a +/- 0.4 V peak signal gives a 0 dB ring signal.

8. Perform the following FRPC TO FRPV ALIGNMENT:

a. Disconnect coaxial inputs at J31 and J32 of FRPV.

b. Jumper TP1 to TP2 in FRPV.

c. Select a modulation mode of CW i.e. 1C1 = 1C2 = L.

d. IF attenuation remains at 5 dB and the LOOP BANDWIDTH is set to 30 Hz, i.e. CBL13-1C7 = 1C6 = H.

e. VCXO sweep is disabled, i.e. CBL13 - 1C5 = 1C4 = H.

f. Configure the input to give a 50 Hz offset frequency.

g. In FRPC make the following adjustment:

1) Set P1 for 15 V peak to peak at pin 6 of U4.

2) Select BPSK modulation mode i.e. CBL13-1C2 = L, 1C1 = H, and set P2 for 15 V p-p at pin 6 of U4.

3) Select QPSK i.e., CBL13-1C2 = H, 1C1 = L, and set P3 for 15 V p-p at pin 6 of U4.

4) Select CW i.e., CBL13-1C2 = 1C1 = L, and set P4 for zero average voltage at TP1. Verify that the average remains zero for all modulations at TP1.

5) With modulation equal to CW set P5 for zero average voltage at TP2.

6) With modulation equal to BPSK check for zero average voltage at TP2.

7) With modulation equal to QPSK, check TP2 for zero average voltage. Adjust P3 for any trim required.

8) Check TP3 to ensure there is 4 V p-p for CW (adjust P1), 2 V p-p for BPSK (adjust by P2), and 1 V p-p for QPSK (adjust P3).

9) Perform the following FRPV ALIGNMENT:

a. Reconnect coax to J31 and J32, leave the jumper installed above, and validate the 8 a. thru f. initial conditions above.

b. Remove any frequency offset inserted above.

c. Set P2 (R36) for 0 V at TP3 (U1 pin 10).

d. Set P3 (R37) so that the measured frequency output of the VCXO (TP7) is 950 kHz +/- 1 Hz. Observe the voltage at TP6. This voltage is the voltage required for the VCXO center frequency.

e. Select scope scale of 2 V per cm and center the idle trace to the center frequency voltage observed in d above. Select maximum deviation by setting CBL13-IC4 = IC5 = L. Select loop bandwidth of 1 kHz by setting CBL13-IC6 = IC7 = L.

f. Adjust P4 so that the voltage at TP6 swings symmetrically about the center frequency voltage (approximately 10 Hz at +/- 5 v).

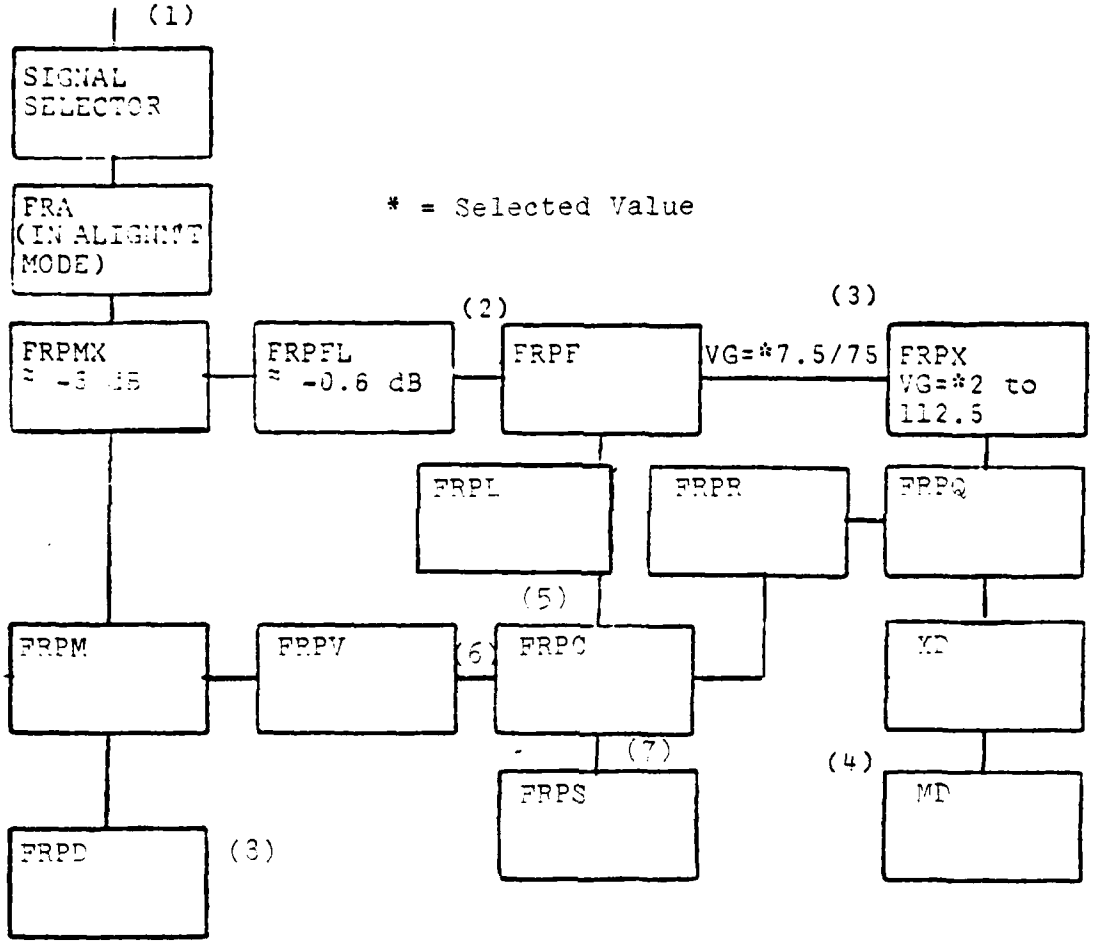
g. Adjust P1 for 10 v p-p at TP6. P4 and P1 may interact, so the adjustment of P1 and P4 should be accomplished with respect to each other.

h. Remove the jumper. Lock should occur in all cases with proper selection of loop bandwidth and IF bandwidth.

APPENDIX F

NOMINAL LEVELS

The following diagram displays the nominal operating levels for the Frequency Receiver.



(1) TEST: -55dBm; FULL SCALE: -47dBm @ 80 MHz
(2) TEST: -3.6 dBm; FULL SCALE: +4.4 dBm INTO 50Ω @ 50 MHz
(3) TEST: 1.12 VRMS; FULL SCALE: 2.81 VRMS
(4) TEST: +0.16 V peak; FULL SCALE: ±0.40 V peak
(5) 1.5V peak sine wave
(6) CW: 4V p-p; PSK: 2 V p-p; QPSK: 1 V p-p when FRPV disconnected & shorted
(7) 4 V p-p open loop 2 V DC when in lock
(3) 95 MHz; @ + 16 dBm

APPENDIX G

COMPUTER MENUS

This appendix addresses the significant computer menus which interface the operator and the Frequency Receiver system. Also discussed are the software requirements which support this operation.

ctrl035 - MODIFY FREQ RCVR OPERATION - FREQ RCVR -

MODULATION	CW a	NORMAL PSK b	QPSK c	OPEN LOOP d
IF BANDWIDTH (kHz) (greater than data rate)	0.2 e	3 f	10 g	30 h
LOOP BANDWIDTH (Hz) (less than data rate)	30 l	100 m	300 n	1000 o
SWEEP DEVIATION (Hz)	OFF r	+/- 200 t	+/- 500 u	+/- 1000 v
This FR to MOD DISPLAY. MODLTN DISPLY w	0.1 x	1 y	10 z	PREV MENU ß
FREQ CNTR gate (sec)				

HELP MENU - MODIFY FREQ RCVR OPERATION

MODULATION:

These buttons select the type of modulation that is desired for display. Open Loop is normally used when the system is in a test mode.

IF BANDWIDTH (kHz):

These buttons select one of the four possible IF filters. For good results choose IF bandwidths so that the expected data rate (in BPS) is less than the selected IF bandwidth (in kHz).

LOOP BANDWIDTH (Hz):

These buttons select which one of the four possible loop bandwidths will be selected for Frequency Receiver operations. Normally the loop bandwidth must be less than the data rate.

SWEEP DEVIATION:

These buttons select the sweep deviation magnitude (or presence). This sweep waveform is used to cause the

Frequency Receiver to search for signals when the receiver is not IN LOCK.

FREQUENCY COUNTER GATE TIME:

These buttons select the gate time of the Frequency Counter. This gate time impacts on the counters accuracy.

REQUIRED ACTIONS:

All entries from this menu are optional replacements for default selections from prior menus. Normal selections should be guided by the data rate to IF and Loop bandwidth relationships stated above.

SOFTWARE NOTES - MODIFY FREQ RCVR OPERATION (CTRL035)

BUTTON TITLE:

MODULATION:

These buttons are used in place of the default options for modulation selection. Identify which button was pushed and activate the appropriate CB.

CONTROL BIT: CBL 9; 1C2, 1C1

MODULATION	1C2	1C1
CW	L	L
BPSK	L	H
QPSK	H	L
OPEN LOOP	H	H

BUTTON TITLE:

IF BANDWIDTH (kHz):

These buttons select the receiver IF bandwidths. Decode the selected button per the following table.

CONTROL BITS: 0C1, 0C0

BANDWIDTH	3C1	3C0
200 Hz	H	H
2 kHz	H	L
10 kHz	L	H
30 kHz	L	L

BUTTON TITLE:

LOOP BANDWIDTH:

These buttons select the PHASE LOCK LOOP BANDWIDTHS. Identify which button was selected and decode as below.

CONTROL BITS: CBL 9; 1C7, 1C6

LOOP BW	1C7	1C6
30	H	H
100	H	L
300	L	H
1000	L	L

BUTTON TITLE:

SWEEP DEVIATION:

These buttons turn off the VCXO SWEEP or modify its magnitude. This magnitude then impacts upon the receiver search range.

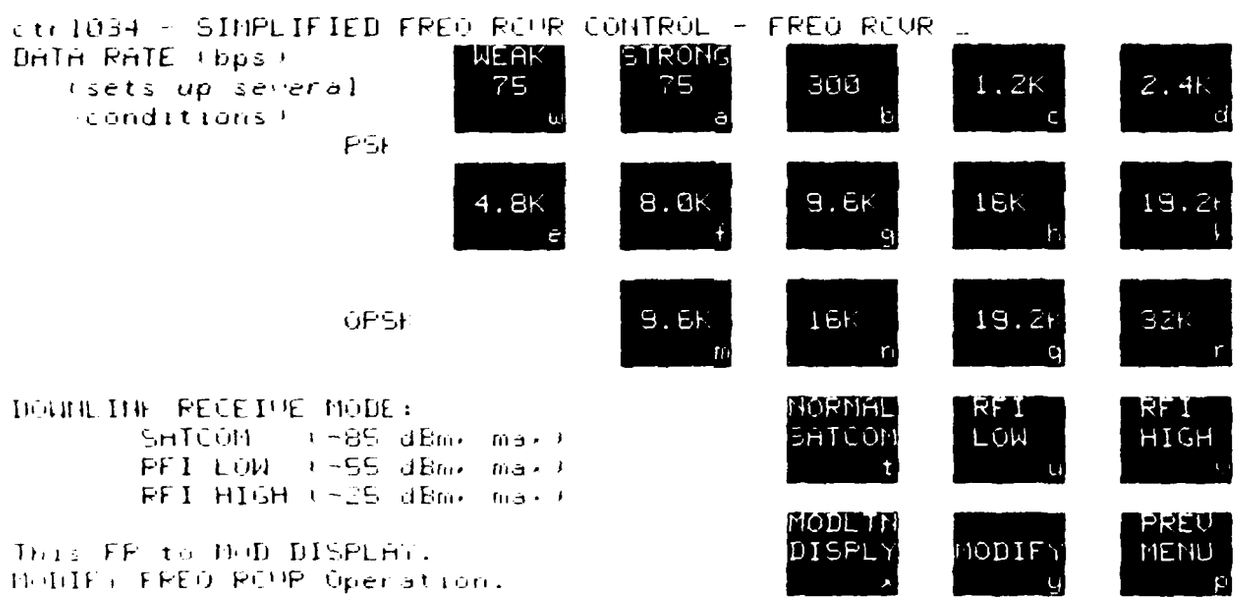
CONTROL BITS: CBL 9; 1C5, 1C4

SEP DEV (Hz)	1C5	1C4
OFF	H	H
+/- 200	H	L
+/- 500	L	H
+/- 1 K	L	L

BUTTON TITLE:

FREQUENCY COUNTER GATE TIME:

These buttons direct the PDP-11 to output on the IEEE bus the appropriate gate set-up command to the HP Frequency Counters. Record which GATE TIME is required (eg. 0.01, 0.1, 1, or 10), and output the proper decoded instruction.


ctr 1034 - SIMPLIFIED FREQ RCVR CONTROL - FREQ RCVR _
DATA RATE (bps)
(sets up several conditions)
WEAK 75 w
STRONG 75 a
300 b
1.2K c
2.4K d
PSK
4.8K e
8.0K f
9.6K g
16K h
19.2K i
QPSK
9.6K m
16K n
19.2K o
32K r
DOWNLINK RECEIVE MODE:
SATCOM (-85 dBm, max)
RFI LOW (-55 dBm, max)
RFI HIGH (-25 dBm, max)
NORMAL SATCOM t
RFI LOW u
RFI HIGH v
This FP to MOD DISPLAY.
MODIFY FREQ RCVR Operation.
MODIFY DISPLY x
MODIFY y
FREQ MENU p

HELP MENU - SIMPLIFIED FREQUENCY RECEIVER CONTROL

DATA RATE (bps):

These buttons set up pre-selected combinations of Frequency Receiver options.

MODE

The selection of the type of Frequency Receiver Mode determines the amount of receiver gain. Selection of the type of mode depends upon the expected signal strength. The SATCOM MODE is the normal operating mode. This mode is selected when signals are expected to be in the range from -85 dBm to -140 dBm. The RFI LOW MODE is to be selected when signals are expected to be in the range from -55 dBm to -110 dBm. The RFI HIGH MODE is to be selected when signals are expected to be in the range from -25 dBm to -80 dBm.

MODIFY FREQ RCVR OPERATION:

Selection of this button allows the operator to call the menu that allows him to specifically change Frequency Receiver modulation type, IF bandwidth, Loop bandwidth, VCXO sweep deviation, and Frequency Counter gate time.

REQUIRED ACTION

Select either PSK data rate or QPSK data rate. Select MODE contingent upon anticipated signal strength. Select MODIFY FREQ RCVR if non-standard configurations are required.

SOFTWARE NOTES - SIMPLIFIED FREQ RCVR CONTROL (CTRL034)

BUTTON TITLE:

DATA RATE (BPS):

Identify which of the buttons have been pushed. Use this entry to enter the applicable table below. If PSK data rate is selected, set 1C2 - L and 1C1 = H. If QPSK data rate is selected, set 1C2 = H and 1C1 = L.

CONTROL BITS: CBL 9; 1C7, 1C6, 1C2, 1C1, 0C1, 0C0

LOOK-UP TABLE FOR ENTRY BY PSK DATA RATE SELECTION

DATA RATE	LOOP BW	= 1C7	1C6	IF BW	= 0C1	0C0
75	30	H	H	3K	H	L
300	100	H	L	3K	H	L
1.2K	300	L	H	3K	H	L
2.4K	300	L	H	3K	H	L
4.8K	1K	L	L	10K	L	H
8.1K	1K	L	L	10K	L	H
9.6K	1K	L	L	30K	L	L
16K	1K	L	L	30K	L	L
32K	1K	L	L	30K	L	L

LOOP-UP TABLE FOR QPSK DATA RATE SELECTION

DATA RATE	LOOP BW =	1C7	1C6	IF BW =	0C1	0C0
9.6K	1K	L	L	30K	L	L
16K	1K	L	L	30K	L	L
19.2K	1K	L	L	30K	L	L
32K	1K	L	L	30K	L	L

BUTTON TITLE:

MODE:

The SATCOM MODE is the normal operating mode. This mode is selected when signals are expected to be in the range from -30 dBm to -120 dBm. The RFI LOW mode is to be selected when signals are expected to be in the range from -55 dBm to -110 dBm. The RFI HIGH mode is to be selected when signals are expected to be in the range from -25 dBm to -80 dBm. Record which of the modes were selected and insert the following attenuators.

CONTROL BITS: CBL 9; 1C0, 0C7, 0C6, 0C5, 0C4, 0C3, 0C2

MODE	CIB SETTING
RFI HI (65 dB total)	1C0 = 0C7 = 0C3 = L 0C6 = 0C5 = 0C2 = 0C4 = H
RFI LO (66 dB total)	1C0 = 0C7 = 0C4 = L 0C6 = 0C5 = 0C3 = 0C2 = H
SATCOM	0C5 = 0C3 = L 1C0 = 0C7 = 0C6 = 0C4 = 0C2 = H (5 dB)

BUTTON TITLE:

MODIFY FREQUENCY OPERATION:

This button is used when the operator desires to initiate Frequency Receiver modifications of a more sophisticated level than those default options above. Software should tab to menu CTROL035 - MODIFY FREQ RCVR OPS for the appropriate receiver that has been selected (ie. FR1 or FR2).

CONTROL BITS: none

APPENDIX H

MODULE SUMMARY

This appendix provides a working summary of each of the Frequency Receiver modules.

MODULE DESCRIPTOR

NAME: FRPC (Frequency Receive-PLL;Carrier Recovery)

FUNCTION:

The Carrier Recovery Module recovers the carrier of a signal. In the recovery process for phase modulated binary signals (BPSK) a doubler is used. For quadriphase signals a quadrupler is used. An lock status signal is also developed and sent to FRPS for processing.

MAXIMUM INPUTS:

J21 (from FRPL J20) = 1.2 V peak

J28 (from FRPR J29) = TTL

J27 (from FRPR J30) = TTL

OUTPUT LEVELS:

J25/26 : 4 V P-P IN OPEN LOOP; 2 V DC WHEN IN-LOCK

J23/24 : 4 V P-P FOR CW; 2 V P-P FOR BPSK; 1 V P-P FOR QPSK

(FRPV DISCONNECTED AND SHORTED)

CONTROL BITS: 1C1(3C1); 1C2(3C2)

Pin/CB	Pin/CB	Connects	Mode Selected
9/1C1	10/1C2		
0	0	13 to 12;3 to 1	QPSK
0	1	13 to 14; 3 to 5	QPSK
1	0	13 to 15; 3 to 2	BPSK
1	1	13 to 11; 3 to 4	CW

MODULE DESCRIPTOR

NAME: FRPD (Frequency Receiver-PLL; Divider)

FUNCTION:

This module accepts 95 MHz sinusoid as an SSA provided input and divides it by 100 to provide 95 kHz TTL as an output. This output is used in the open loop mode to act as a non-coherent substitute for the VCXO. Output presence is dictated by control bits. Under some circumstances (i.e. closed loop operations) output will cease.

MAXIMUM INPUTS:

J10 = sinusoid (95 MHz) at + 15 dBm

GAINS: none CONTROL BITS: 1C1(3C1);1C2(3C2)

Both bits must be HI (= + voltage) to inhibit output.

MODULE DESCRIPTOR

NAME: FRPF (Frequency Receiver-PLL; Filter Bank/Amplifier)

FUNCTION:

This module routes the incoming signal to one of four digitally selected IF filters. The first 50 kHz signal amplification is also accomplished in this module. Analog information is also provided to FRPX.

OUTPUTS:

J17 = sinusoid at approximately 50 kHz to FPRL

J16 = sinusoid at approximately 50 kHz to FRPX

MAXIMUM INPUTS: approximately 0 dbm (223 mv rms) to J13

GAINS:

J13 to J17 voltage gain = 53

J13 to J16 voltage gain = 7.5 or 75

CONTROL BITS:

CBL13 - 0C1 (2C1), 0C0 (2C0)

CBL15 - 2C7

(Negative Logic) 0C1	0C0	BANDWIDTH
0	0	200 Hz
0	1	3 kHz
1	0	10 kHz
1	1	30 kHz

2C7

1 = 7.5 voltage gain

0 = 75 voltage gain

MODULE DESCRIPTOR

NAME: FRPL (Frequency Receiver-PLL; Limiter/Filter)

FUNCTION:

This module accepts input signals at 50 kHz from FRPF. It provides sufficient gain and amplitude limiting action so that its output amplitude is essentially constant and independent of received signal level. After filtering the sinusoidal output is routed to FRPC for use in phase detection and carrier recovery.

MAXIMUM INPUTS:

15 v p-p at J19

GAINS:

N/A - output level = 1.5 v peak regardless of input level.

CONTROL BITS: none

MODULE DESCRIPTOR

NAME: FRPM (Frequency Receiver-PLL: Mixer Driver)

FUNCTION:

This module performs three functions:

1. It switches between VCXO generated frequencies and the 950 kHz generated in the open loop mode by FRPD. The selected input is then inverted to produce a pair of TTL signals 180 degrees out of phase with each other. This pair of signals is then passed through a high current gate and transformer combination which produces the necessary +17 dBm at 50 ohms to drive the 1 MHz to 50 kHz down-converter.

2. A sample of the selected frequency source is made available to the Frequency Counter (FC).

3. Control bit CBL13-1C0 is inverted, then passed thru a ULN2003A which is a 28 V current driver which operates the solenoid in the 32 dB Daico (single step) attenuator.

MAXIMUM INPUTS:

J34 = 950 kHz (+/- 1 kHz) TTL from FRPV

J39 = 950 kHz TTL from FRPD

J40 = control bit (TTL) 1C0

GAINS: none

CONTROL BITS: CBL13-1C1, 1C2

132	131	SELECTS
0	0	Open Loop
0	1	VCXO
1	0	VCXO
1	1	VCXO

<NEGATIVE LOGIC>

MODULE DESCRIPTOR

NAME: FRPQ (Frequency Receiver-PLL; Quadriphase Mixer)

FUNCTION:

This module accepts a 50 kHz analog signal from FRPX. This input is processed with reference frequencies from FRPP to generate the display for MD. After low-pass filtering, the resultant phase information is amplified to produce a pair of +/- 0.68 V signals at 50 ohms which are applied to the X and Y inputs of the X-Y display.

MAXIMUM INPUTS:

Full scale = 5.62 vrms		-44 dBm at Signal Selector input
Test	= 2.24 vrms	-55 dBm at Signal Selector input

GAINS:

N/A

CONTROL BITS: none

MODULE DESCRIPTOR

NAME: FRPR (Frequency Receiver-PLL; Reference Frequency Generator)

FUNCTION:

This module accepts the SSA system derived 800 kHz standard TTL reference frequency. The function of this module is to produce a two phase, coherent, 50 kHz TTL reference signal whose phase relationship is precisely 90 degrees apart. This pair of signals serves as reference input levels to the X-Y driver. FRPR also produces two reference TTL level signals 90 degrees apart for phase comparison to incoming signals in FRPC. The frequency of these signals is digitally selected in accordance with the selected/desired type of modulation, ie. CW, BPSK, QPSK.

MAXIMUM INPUTS:

J2 = TTL (+/- 5 VDC)

GAINS: N/A

OUTPUTS:

J5 - 50 kHz angle 90 - phi

J6 - 50 kHz angle 0 - phi

J29 - 50, 100, or 200 kHz angle 90 - phi

J30 - 50, 100, or 200 kHz angle 0 - phi

CONTROL BITS: 1C1(3C1);1C2(3C2)

1C2	1C1	MODULATION/FRQ SELECTED
0	0	QPSK - 200 kHz
0	1	QPSK - 200 kHz
1	0	BPSK - 100 kHz
1	1	CW - 50 kHz

MODULE DESCRIPTOR

NAME: FRPS (Frequency Receiver-PLL; Status)

FUNCTION:

The Status Module accepts input from the Carrier Recovery module and provides outputs to the X-Y display (in or not in lock), the computer (in or not in lock), and an external gate enable to the configured frequency counter. This in lock status is also sent to FRPV and is used to disable the VCXO control ramp generator.

NOMINAL INPUTS:

4 v p-p open loop (if signal is present)

2 v dc when in lock

GAINS:

N/A

CONTROL BITS:

None

MODULE DESCRIPTOR

NAME: FRPV (Frequency Receiver-PLL; VCO and PLL)

FUNCTION: This module accepts phase signal information from FRPC and after loop filtering derives an error voltage which is summed with a sweep frequency and a control voltage to a Voltage Controlled Crystal Oscillator (VCO). Also contained in this module is a triangle ramp generator which responds to an enable signal generated in the FRPS module reflecting lock status. The sweep is enabled when the receiver is out of lock. Sweep amplitudes (deviations) and speeds (rates) are digitally selectable. This module also contains loop filters with digitally selectable bandwidths.

MAXIMUM INPUTS: J31 - +/- 5 V from FRPC

GAINS: none

OUTPUT: 950 kHz +/- 1 kHz at J36

CONTROL BITS: 1C7(3C7);1C6(3C6);1C5(3C5);1C4(3C4)

1C7	1C6	LOOP BANDWIDTH (NOMINAL)
0	0	30 Hz
0	1	100 Hz
1	0	300 Hz
1	1	1 kHz

1C5	1C4	RAMP DEVIATION
0	0	OFF
0	1	+/- 1 V
1	0	+/- 2.5 V
1	1	+/- 5 V

MODULE DESCRIPTOR

NAME: FRPX (Frequency Receiver-PLL; X-Y Attenuator)

FUNCTION:

This module conditions the 50 kHz signal output from FRPF and produces a useable signal for the X-Y display. Gain through this module is digitally adjusted and controlled by the computer in 5 dB steps over a range of 35 dB.

MAXIMUM INPUTS:

J16 : 2.81 v rms

GAINS: J16 to J54 - adjustable voltage gain 2 to 112.5 in 5 dB steps.

CONTROL BITS: (X-Y Control Byte) 2C6,2C5,2C4

2C6	2C5	2C4	GAIN	DB
0	0	0	0	
0	0	1	5	
0	1	0	10	
0	1	1	15	
0	0	0	20	NOTE : 2C7 = 1 FOR ALL FOLLOWING ENTRIES
0	0	1	25	
0	1	0	30	
0	1	1	35	
1	0	0	40	
1	0	1	45	
1	1	0	50	
1	1	1	55	

LIST OF REFERENCES

1. Naval Postgraduate School Report NPS62-78-002, Receiver Design for the Naval Postgraduate School SATCOM Signal Analyzer, by C. B. Williams and J. E. Ohlson, January, 1978.

2. Rhoades, W. A., Integration of the Primary Receiver into the NAVPGSCOL SATCOM Signal Analyzer, Master's Thesis, Naval Postgraduate School, Monterey, California, June, 1978.

3. Naval Postgraduate School Report NPS62-79-016PR, Frequency Receivers in the Satellite Communications Signal Analyzer, by M. J. Rogers and J. E. Ohlson, December, 1979.

4. Ohlson, J. E., SATCOM Signal Analyzer Design Review, Naval Postgraduate School, Monterey, California, 10 April 1979.

5. Viterbi, A. J., Principles of Coherent Communications, McGraw Hill, 1966.

6. Lindsey, W. C., Phase-Locked Loops & Their Applications, IEEE Press, 1977.

7. Jaffe, R., Rechtin, E., Design and Performance of Phase-Lock Circuits Capable of Near-Optimum Performance Over a Wide Range of Input Signal & Noise Levels, IRE Trans. Inform. Theory, Vol. IT-1, pp. 60-67, March 1965.

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-8